An *E*-Band Analog Predistorter and Power Amplifier MMIC Chipset

Marcus Gavell, Göran Granström, Christian Fager, Sten E. Gunnarsson, Mattias Ferndahl, and Herbert Zirath

***Abstract*— An analog predistorter and power amplifier (PA) MMIC chipset has been designed to improve the overall linearity for applications in wireless communication at the *E*-band. The circuits have been implemented in a commercial 0.1 μm InGaAs pHEMT process. The PA delivers an output referred 1-dB gain compression ($OP_{1\ dB}$) of 24 dBm, saturated output power of 27 dBm, and OIP3 of 32 dBm between 71 and 76 GHz. In combination with the analog predistortion circuit, the combined chipset improves carrier to third-order intermodulation ratio by 20 dB at an average output power of 21 dBm and at the same time increasing the $OP_{1\ dB}$ by 2 dB to 26 dBm.**

***Index Terms*— Analog, analog predistorter (APD), GaAs, linearization, MMIC, predistortion (PD), pHEMT, power amplifier (PA), predistortion.**

I. Introduction

THE increasing use of mobile data services has rocketed the data traffic in the mobile backhaul networks. While many traditional microwave frequency bands suffer from low capacity and congested deployment, the *E*-band (71–76 and 81–86 GHz) has proven to deliver high data-rates, making it the preferred point-to-point frequency band to use in the mobile backhaul networks [1]. Today, several radio manufacturers have demonstrated wireless data rates exceeding 10 Gb/s using wide bandwidths and complex modulation formats [2], [3]. Despite of having higher spectral efficiency, complex modulation format has two disadvantages: 1) higher peak-to-average-ratio and 2) tougher requirements on spectral emissions. Both effectively contribute to decrease the transmitter's output power and consequently its efficiency. Present power amplifiers (PAs) must be backed off significantly from their peak power in order to operate linearly and comply with the spectral emission mask.

Linearization techniques are commonly utilized at narrow bandwidth applications to allow the use of less linear but more efficient PAs. It also gives the opportunity to operate the PAs closer to their peak power, increasing the operational efficiency even further. In the majority of these cases, linearization techniques are implemented in the digital domain at the expense of increased bandwidth in the baseband modem, known as digital predistortion (DPD). At the *E*-band, the signal bandwidth can be significantly large, up to 5 GHz, requiring very high sample rates, multiple times the signal bandwidth for implementing DPD [4]. On the contrary, the analog predistortion (APD) of PAs can be implemented with negligible power consumption to enhance the linearity over large bandwidths without the need for increasing the sample rate in the modem [5]. The work in [6] presents the simulations and improvements of using a GaAs APD for linearizing traveling wave tube amplifiers at the *E*-band and *W*-band. In [7], a varactor is used to linearize the nonlinear gate–source capacitance and in [8] and [9], a cold FET and antiparallel diodes are used to form gain expansion, respectively. The APD in this letter relies on the gain expansion characteristics from a Class C amplifier. We present the designs of the first GaAs APD and PA chipset at the *E*-band and the comparison of measurement results for the standalone PA and the combined APD + PA.

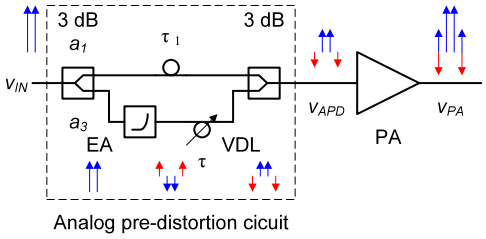

Fig. 1. Concept to generate and cancel the IM3 product.

II. Concept

The concept of predistortion is to compensate for the nonlinearities generated by the PA *a priori*, regardless if this is performed in the digital or analog domain. It also means that, in principle, all intermodulation (IM) products (third, fifth, ...) can be taken into account and canceled [9]. In this letter, the APD is designed to compensate for the dominant third-order IM (IM3) product.

Fig. 1 shows the lineup and function of the APD and PA. The cancellation of the IM3 product is illustrated in Fig. 1 using two-tone excitation and is explained mathematically in (1) using a third order polynomial model. The linearization works as follows: The APD circuit generates in the lower branch an IM3 product from the cubic term ($a_3 v_{\mathrm{IN}}^3$ in (1)) such that, after amplified by the PA (g_1), has the same amplitude ($g1\, a_3$) but is out of phase of the PA generated IM3 product ($g_3\, a_1^3$). The two IM3 contributions add destructively at the output of the PA such that the PA is linearized

$$\begin{aligned} v_{\mathrm{APD}}(v_{\mathrm{IN}}) &= a_1 v_{\mathrm{IN}} + a_3 v_{\mathrm{IN}}^3 \\ v_{\mathrm{PA}}(v_{\mathrm{APD}}) &= g_1 v_{\mathrm{APD}} + g_3 v_{\mathrm{APD}}^3 \\ v_{\mathrm{PA}}(v_{\mathrm{IN}}) &= a_1 g_1 v_{\mathrm{IN}} + (g_1 a_3 + g_3 a_1^3) v_{\mathrm{IN}}^3 + \cdots \end{aligned} \quad (1)$$

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III. Circuit Design

The APD and PA circuits have been implemented in WIN Semiconductors PP10-10 InGaAs 0.1 μm pHEMT technology with 50-μm wafer thickness. For a 2×75 μm-wide-transistor, the process' typical electrical parameters are 135/200-GHz transition frequency (f_T) and maximum oscillation frequency ($f_{\max}$), respectively. The saturation current ($I_{D,\max}$) is 760 mA/mm and saturated power density of 850 mW/mm [10]. This III–V process features front and backside metalization, through substrate vias, 50 $\Omega/\square$ thin film resistors and 400 pF/mm^2 Metal Insulator Metal capacitors.

The APD circuit consists of two branches, one linear branch (a_1) and one nonlinear branch (a_3), divided and combined with 3-dB Wilkinson power combiners, shown in Fig. 1. The nonlinear branch uses a Class C error amplifier (EA) as the source to the cubic term $a_3 v_{\text{IN}}^3$. This term features strong appearance in Class C and is positive in contrast to a Class AB biased transistor [9]. The linear branch consists of a fixed delay line (τ_1) to match the delay of the nonlinear branch. In order to achieve $g_1 a_3 + g_3 a_1^3 = 0$, such that the IM3 component is canceled at the output of the PA, the amplitude of a_3 is controlled by the gate bias (V_{G1}) of the EA and the phase from the variable delay line (VDL) is controlled by V_{G2}. The limited tuning range of a_3 bounds, in this case the combination of PAs, to have similar gain and linearity as the PA described in the next paragraph. The VDL consists of two lumped transmission line Pi-sections from varactors C_3 and inductors L_2. In total, the delay can be adjusted ± 1 ps. A schematic of the APD is shown in Fig. 2(a) and a photograph of the APD MMIC in Fig. 2(b).

In Fig. 2(c), a photograph of the designed PA is shown. It is a four parallel and four stage amplifier design. The gate widths of the first to final stage are 300, 400, 800, and 1200 μm, biased at 0.25 A/mm and 3.3 V. The gradual increase in gate width from the first to the last stage is a design compromise between efficiency, output power, gain, and linearity. The four parallel branches are divided and combined with tee-junctions for minimizing loss. Because there is no isolation between the branches, the combining network was synthesized with common-mode excitation in order to provide the optimum load impedance of the transistors.

IV. Results

The circuit verification was performed in two parts: 1) on-wafer probed measurements using one- and two-tone excitation and 2) measurements using modulated signals with the PA and APD + PA mounted and bonded into a fixture with WR12 waveguide interfaces.

The one- and two-tone measurement setup used two Agilent 83620B signal generators together with two $\times 6$ frequency multipliers and electronically controlled attenuators to adjust the power level. The two sources were combined with a 3-dB WR12 hybrid from Flann Ltd. An Agilent E4407B spectrum analyzer and an Agilent 11 970-W harmonic mixer with 50-dB attenuation were used to measure the IM products. The high attenuation is necessary for reducing the IM contribution from the mixer.

In Fig. 3, the APD's tunability was tested by adjusting the control voltages V_{G1} and V_{G2} in order to find the optimum linear condition for the APD + PA. The parameter adjustment makes it possible to adapt for changes in, for instance, process variations, temperature, and signal characteristics. Improvements at different output power levels were observed for

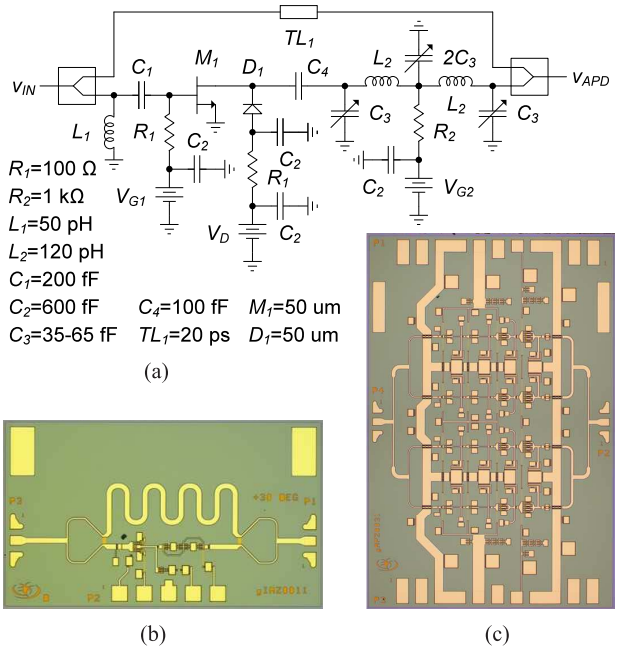

Fig. 2. (a) Schematic representation of the APD circuit. Chip photographs of the (b) E-band APD and (c) PA MMICs. The APD circuit measures 2×1.6 mm^2 and the PA measures 2×3 mm^2 in size, respectively.

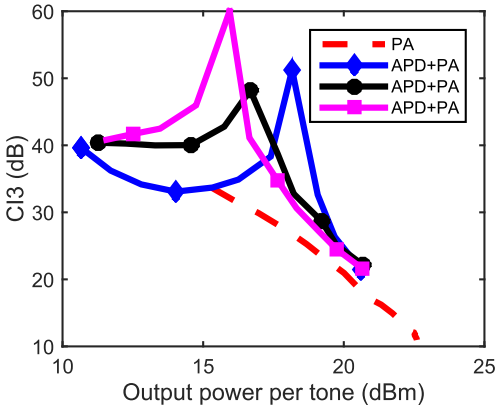

Fig. 3. Measured CI3 versus output power per tone at 10-MHz tone separation frequency and 73.5 GHz center frequency.

$\diamond$: $V_{G1} = -1.35$ V and $V_{G2} = 1.3$ V and $\square$: $V_{G1} = -1.4$ V and $V_{G2} = 0.8$ V and $\circ$: $V_{G1} = -1.4$ V and $V_{G2} = 0.7$ V. In all cases, V_D was fixed at 3.3 V.

The measured gain compression of the PA and the APD+PA is shown in Fig. 4. The PA measures small signal gain of 26- and 1-dB gain compression point ($P_{1\text{ dB}}$) at 24-dBm output power. The combined APD + PA, measures slightly over-compensated $P_{1\text{ dB}}$ of 26 dBm, an improvement of 2 dB. The 8-dB lower gain emanates from the APD's insertion losses (power combiners $\sim$7 dB, delay line $\sim$0.5 dB, and bondwire $\sim$0.5 dB). The simulated AM–PM of the APD + PA shows improved phase error response in compression by approximately 3 °. The lower gain and the EA's dc power dissipation at high input power levels, contribute to lower the PAE to 20% for the combined APD + PA, a reduction by 2%.

In Fig. 4, the carrier to third-order IM (CI3) is plotted versus output power per tone. In comparison to the PA, the combined APD + PA improves the CI3 up to 20 dB at 18 dBm per tone output power.

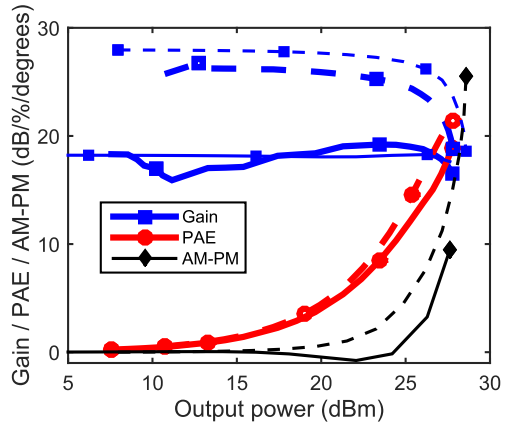

Fig. 4. Measured (thick lines) and simulated (thin lines) gain (□), AM–PM (◇) and PAE (○) versus output power at 73.5 GHz. The APD + PA is plotted in solid lines (-) and the PA is plotted in dashed lines (- -).

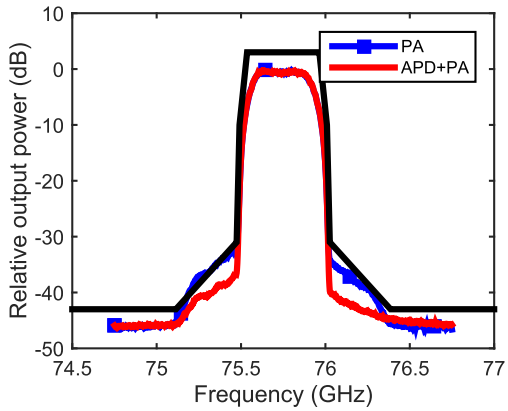

Fig. 5. Measured output spectrum from a 64-QAM-modulated signal with 250-MHz modulation bandwidth at 17-dBm average output power. The mask follows ETSI EN 302-217-2.

In the measurement with modulated signals, an *E*-band transmitter and a modem with symbol rate of 166-MS/s and 64-QAM-modulation pattern were used. In Fig. 5, the measured results show an improvement in the adjacent channel power ratio (ACPR) of 5 dB with the combined APD + PA.

V. Comparison

In Table I, the combined APD + PA and the PA are compared for $P_{1\ \mathrm{dB}}$, saturated output power (P_{SAT}), power added efficiency (PAE), and chip size at the *E*-band with the state-of-the-art PAs. To the best of our knowledge, neither linearized *E*-band GaAs nor GaN PAs exist in the open literature. For this reason, the comparison is conducted with the highest performing GaAs and GaN PAs [11], [12] and linearized PAs in CMOS and SiGe technology, [7], [8], [13]. The work in [7], [8], and [13] shows an improvement of linear output power between 2 and 3 dB when linearization is applied. The presented linearization method improves the linear output power range to 26 dBm, an increase by 2 dB, and improved CI3 by 20 dB at an average output power of 21 dBm. The combined APD + PA and the PA present the highest PAE of the PAs in the comparison, 20% and 22%, respectively. This makes especially the combined APD + PA an efficient component to use in a radio transmitter because of its enhanced ACPR.

TABLE I
Comparison of Linearized and High Performance PAs at the *E*-Band

	[11]	[12]	[7]	[13]	[8]	PA	APD+PA
Frequency (GHz)	71-76	71-76	68-78	60	58-67	71-76	71-76
Gain (dB)	14	17	21.4	1.8	10	26	18
$P_{1\mathrm{dB}}$ / P_{SAT} (dBm)	33/35	27/29	14/17	11/12	10/11	24/27	26/27
PAE (%)	14	15	18.9	12	11	22	20
Size (mm^2)	1.44	9	0.09	na	0.4	6	9.2
Technology	GaN	GaAs	CMOS	SiGe	CMOS	GaAs	GaAs
f_T/f_{max} (GHz)	na/na	135/200	na	200/na	na	135/200	135/200

VI. Conclusion

This letter presents the design and performance of an MMIC GaAs PA and APD chipset. This is the first presented GaAs APD + PA combination at the *E*-band and demonstrates an increase in linear output power of 2 dB. With the use of 64-QAM-modulated signals, the ACPR is improved by 5 dB at an average output power of 17 dBm, allowing the PA to operate at higher efficiency and to transmit higher output power.

References

[1] N. Heuveldop *et al.*, "Ericsson Mobility Report," Ericsson AB, Technol. Emerg. Business, Stockholm, Sweden, Tech. Rep. EAB-17:005964, Jun. 2017. [Online]. Available: http://www.ericsson.com/mobilityreport and www.ericsson.com/mobility-report

[2] Athens, Greece. (Feb. 2017). *Press Releases: Intracom Telecom Launches New E-Band Radio Offering 10 Gbit/s Capacity*. [Online]. Available: http://www.intracom-telecom.com/en/news/press/press2017/2017_02_13.htm

[3] London, U.K. (Aug. 2016). *Press Release: ELVA-1 Announces Promotion for 10 Gigabit Ethernet Link*. [Online]. Available: http://www.elva-1.com/news_events/a40118

[4] A. Katz, J. Wood, and D. Chokola, "The evolution of PA linearization: From classic feedforward and feedback through analog and digital predistortion," *IEEE Microw. Mag.*, vol. 17, no. 2, pp. 32–40, Feb. 2016.

[5] A. Katz, R. Gray, and R. Dorval, "Truly wideband linearization," *IEEE Microw. Mag.*, vol. 10, no. 7, pp. 20–27, Dec. 2009.

[6] A. Katz, M. Chiappetta, and R. Dorval, "Predistortion linearization to 100 GHz," in *Proc. IEEE Top. Conf. Power Amplif. Wireless Radio Appl.*, Jan. 2013, pp. 34–36.

[7] T. Xi, S. Huang, S. Guo, P. Gui, D. Huang, and S. Chakraborty, "High-efficiency E-band power amplifiers and transmitter using gate capacitance linearization in a 65-nm CMOS process," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 3, pp. 234–238, Mar. 2017.

[8] J.-H. Tsai, C.-H. Wu, H.-Y. Yang, and T.-W. Huang, "A 60 GHz CMOS power amplifier with built-in pre-distortion linearizer," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 12, pp. 676–678, Dec. 2011.

[9] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Norwood, MA, USA: Artech House, 2006.

[10] "Technology Release Procedure (0.1 μm Power pHEMT, PP10-10/20)," WIN Semiconductors Corp., Taoyuan, Taiwan, Tech. Rep., 2011.

[11] A. Brown *et al.*, "High power, high efficiency E-band GaN amplifier MMICs," in *Proc. IEEE Int. Conf. Wireless Inf. Technol. Syst. (ICWITS)*, Nov. 2012, pp. 1–4.

[12] E. Camargo, J. Schellenberg, L. Bui, and N. Estella, "Power GaAs MMICs for E-band communications applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–4.

[13] J. T. Valliarampath and S. Sinha, "Designing linear PAs at millimeter-wave frequencies using Volterra series analysis," *Can. J. Elect. Comput. Eng.*, vol. 38, no. 3, pp. 232–237, May 2015.