A *V*-Band Stacked HEMT Power Amplifier With 25-dBm Saturated Output Power in 0.1-μm InGaAs Technology

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***Abstract*— A stacked high-electron mobility transistor (HEMT) power amplifier (PA) has been designed and implemented in a commercial 0.1-μm InGaAs pHEMT process to increase gain and output power at millimeter-wave frequencies. The stability problem of the stacked HEMT has been analyzed. A new layout of the stacked HEMT for improving the high frequency stability is proposed and used in the PA design. Measurements on the three-stage PA with parallel devices verify the saturated output power of 25 dBm and the maximum power added efficiency of 15% at 61 GHz, which is the highest reported output power of stacked HEMT PAs. The chip size measures 3.2 mm^2 which makes this the most power dense *V*-band amplifier reported from GaAs with 100 mW/mm^2.**

***Index Terms*— FET, GaAs, high-electron mobility transistor (HEMT), MMIC, millimeter wave (mm-wave), power amplifier (PA), stability analysis, stacked, *V*-band.**

I. Introduction

POWER amplifiers (PAs) in the millimeter-wave (mm-wave) frequency spectrum are an area of increasing interests due to many emerging applications in security, telecommunications, and radar. To date, GaAs high-electron mobility transistor (HEMT) is the most used and established technology for mm-wave PAs due to its satisfactory high-frequency performance. The reliability, stable manufacturing, performance, and pricing of GaAs are very competitive, which make this technology very attractive for commercial use.

GaAs and other related low-bandgap materials used in processes aimed for mm-waves must operate at relatively low voltages. This limits their ability to generate high output power. Usually, GaAs HEMT processes targeted for mm-wave circuits can operate at a maximum drain voltage of 3.5–4 V. To generate significant output power, these materials need large devices with high current to compensate for the lower operating voltage. However, large devices have worse high-frequency performance and low output impedance, which makes them unfavorable for use in high-frequency PAs.

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Stacking transistors are an interesting concept to develop the GaAs circuit technology toward higher output powers, since it increases the operating voltage of the cell and, therefore, allows for higher voltage swing for the same current. This is satisfied when the gate–source (v_{GS}) and drain–source (v_{DS}) voltage swings of the common-source (CS) and the following stacked transistors are equal. Stacked transistors also occupy a relatively small area compared with the traditional power combining techniques; thus requiring less chip area for a given output power. This makes the higher output power from the stacked HEMT amplifiers more price competitive. Furthermore, the stacked HEMT, which has similarities to the cascode, provides better high-frequency characteristics and higher output impedance than a CS transistor. Reference [1] shows how to optimize the voltage swing of the CS and the stacked transistors to equally distribute the v_{GS} and v_{DS} voltage swings and thereby maximize the output power. This concept is of interest for mm-wave PAs in low-voltage silicon nodes and has been implemented with improved output power [2], [3]. Similarly, stacked HEMTs at mm-wave frequencies in GaAs show successful implementation with improved output power [4], [5]. The concept has good prospects, but the configuration of the stacked HEMT is prone to instability. Circuits based on stacked HEMTs, including cascodes, are difficult to design for this reason. In this paper, we address and analyze the cause of the instability related with the stacked HEMT and propose a layout with improved stability and high-frequency characteristics. We present the design of a stacked HEMT PA at *V*-band based on this layout.

II. Circuit Design

The circuit schematic in Fig. 1 shows the two parallel branches and three-stage PA design. The parameters are shown on one side of the symmetry line and the component values are listed in Table I, including the transistor sizes. The total gate width of the first stage is 200 μm and reaches 600 μm at the final stage. The increasing gate width from the first to the last stage improves efficiency and gain, in comparison to using the same sized transistors and power splitting. The aggregated power along the amplifier also justifies this choice.

Fig. 1 shows how the bias runs vertically across the chip. This will allow for further paralleling of the amplifier cell *N* times if needed. It is also shown that the first two stages are biased from V_{D1} and the final stage is biased separately

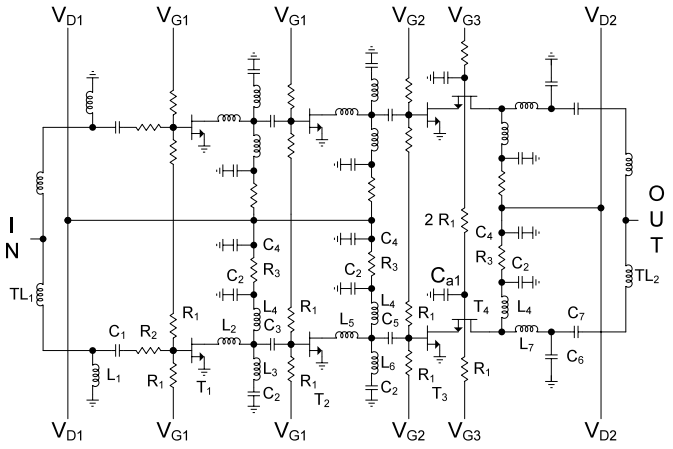

Fig. 1. Schematic of the stacked HEMT PA.

TABLE I
COMPONENT VALUES USED IN THE CIRCUIT DESIGN

Parameter	Value
R_1	1 kΩ
R_2	5 Ω
R_3	2 Ω
$L_{1,5,6,7}$	70 pH
L_2	50 pH
L_3	90 pH
L_4	120 pH
C_1	120 fF
C_2	500 fF
C_3	80 fF
C_4	4 pF
C_5	70 fF
C_6	40 fF
C_7	160 fF
C_{a1}	100 fF
TL_1	71 Ω @ $\lambda/4$
TL_2	55 Ω @ $\lambda/4$
T_1	2 × 50 μm
T_2	2 × 62.5 μm
T_3	6 × 50 μm
T_4	4 × 75 μm

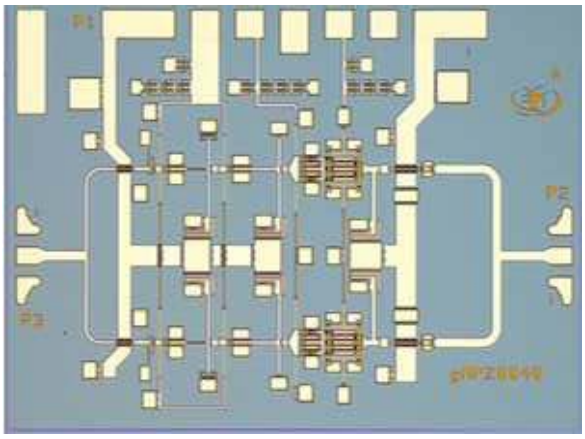

Fig. 2. Layout of the stacked HEMT PA. The chip size measures 2×1.6 mm^2.

from V_{D2}. The current distribution on V_{D1} and V_{D2} is quite uniform due to the total gate width of 450 and 600 μm, respectively. The circuit's layout is shown in Fig. 2.

A. GaAs 0.1-μm pHEMT Technology

The technology being used is WIN Semiconductors PP10-10 InGaAs 0.1-μm pHEMT technology [6]. The typical electrical parameters of the process are 135/200 GHz transition frequency (f_T) and maximum oscillation frequency ($f_{\max}$) for a 2 × 75 μm wide transistor. The current saturation ($I_{D,\max}$) is 760 mA/mm and the saturated power is 850 mW/mm. Furthermore, this III–V process includes the front and backside metallization, vias between the front and backside, 50-Ω/□ thin-film resistors and 400-pF/mm^2 metal–insulator–metal capacitors.

B. Power Optimization

The output network is critical to a PA to deliver maximum output power. In the case of the stacked HEMT, it is equally critical to optimize the load line (LL) of the CS HEMT to equally distribute the voltage swing between the CS HEMT and the second HEMT, identified as T_3 and T_4 in Fig. 1, respectively. The load impedance of the CS HEMT is largely determined by the capacitance C_{a1}. For this reason, C_{a1} is part of the optimization to find $Z_{L,\text{opt}}$. Equally distributing the LLs between the CS HEMT and the stacked HEMT will also positively influence the circuit's reliability. The simulated LLs, time domain waveforms, and voltage swings of v_{DS} and v_{GS} of both stages are shown in Fig. 3.

The maximum delivered output power from a stacked HEMT using low-frequency approximation is derived in [1] and shown in (1). The conditions for delivering maximum output power for equally sized CS HEMT and second HEMT are shown in (2). When applying the conditions for maximum output power (2) in (1), C_{a1} can be determined by the expression given in (3). C_{a1} depends mainly on the gate–source capacitance C_{GS} and the load impedance Z_L. The initial value for C_{a1} can therefore easily be calculated. C_{GS} can be extracted from the transistor model and the optimum load impedance can either be calculated based on the LL trajectory or more accurately found from load–pull data of the CS HEMT. In this specific case, by using the intrinsic parameters $C_{\text{GS}} = 300$ fF, $g_m = 200$ mS, and $g_{\text{DS}} = 0$ S and load impedance $Z_L = 50$ Ω, the extrinsic capacitance C_{a1} is calculated to be 75 fF. Ultimately, C_{a1} needs to be optimized under large signal conditions for achieving maximum output power from the stacked HEMT. During the optimization at 60 GHz, C_{a1} was found to be 100 fF:

$$P_{\text{OUT}} = \Re\left\{\frac{|v_{D2}|}{2}\left(\frac{g_m|v_{\text{GS1}}| + g_m|v_{\text{GS2}}|}{2} + |v_{D2}|\frac{g_{\text{DS}}}{2}\right)\right\} = \Re\left\{\frac{|v_{D2}|^2}{2Z_L}\right\} \tag{1}$$

$$|v_{D2}| = 2|v_{D1}|$$

$$|v_{\text{GS2}}| = |v_{\text{GS1}}| = |v_{D1}|\frac{C_{a1}}{C_{a1} + C_{\text{GS}}} \tag{2}$$

$$C_{a1} = C_{\text{GS}}\frac{2Y_L - 2g_{\text{DS}}}{g_m + 2g_{\text{DS}} - 2Y_L}. \tag{3}$$

The optimum load impedance for the stacked HEMT was found using load–pull simulations with the large signal transistor model in Keysight ADS. In theory, the optimum $Z_{L,\text{opt}}$ for

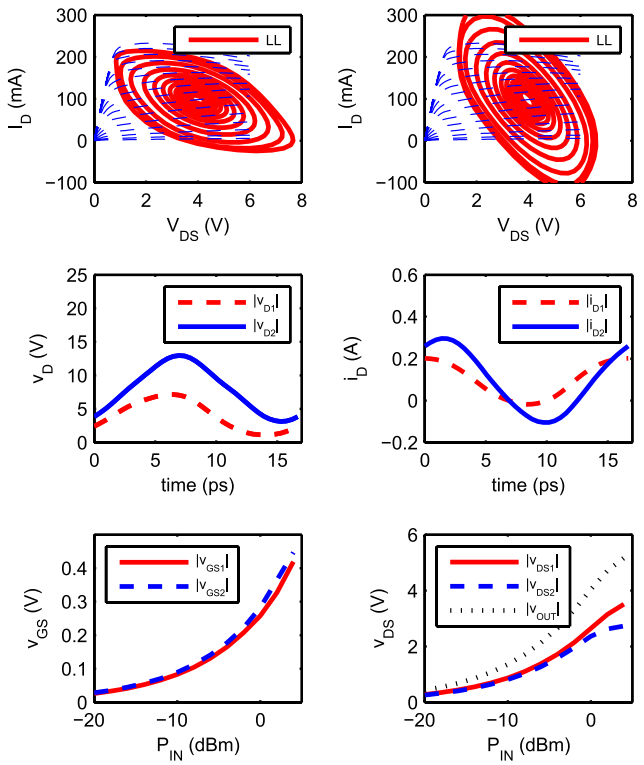

Fig. 3. Simulated intrinsic LLs (red continuous lines) with input power levels from −20 to 4 dBm for the CS HEMT (top left) and for the second HEMT (top right). Simulated time domain intrinsic voltage waveforms of v_{D1} and v_{D2} (middle left) and current waveforms of i_{D1} and i_{D2} (middle right). Bottom left: simulated intrinsic gate–source voltage swings v_{GS1} of the CS HEMT (red continuous line) and v_{GS2} of the second HEMT (blue dashed line). Bottom right: simulated intrinsic drain–source voltage swings v_{DS1} of the CS HEMT (red continuous line), v_{DS2} of the second HEMT (blue dashed line), and v_{out}, the output voltage swing from the stacked HEMT (black line).

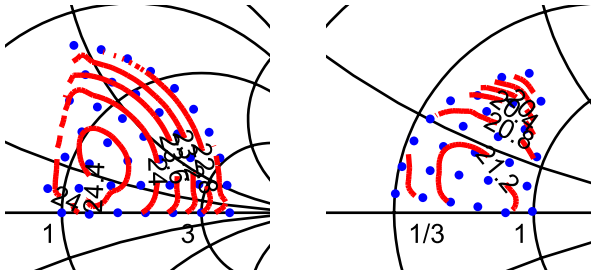

Fig. 4. Contour lines of the measured output power P_{OUT} of the stacked HEMT versus Z_L (red continuous lines) and the sampled Z_L points (blue dots). Left: stacked HEMT. Right: CS HEMT. In the measurement, the input power was 2 dBm. In both plots, the normalized impedance is $Z_0 = 50\ \Omega$.

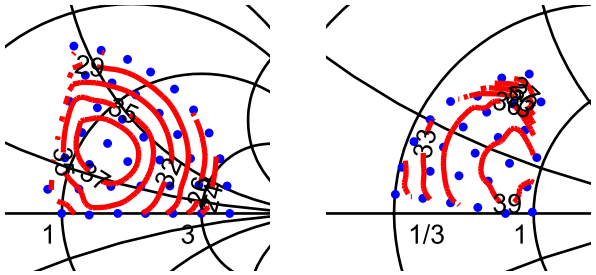

Fig. 5. Contour lines of the measured PAE of the stacked HEMT versus Z_L (red continuous lines) and the sampled Z_L points (blue dots). Left: stacked HEMT. Right: CS HEMT. In the measurement, the input power was 2 dBm. In both plots, the normalized impedance is $Z_0 = 50\ \Omega$.

the stacked HEMT shall double for the same gate width. The load impedances for the $6 \times 50\ \mu$m CS HEMT and the stacked HEMT at 60 GHz were found to be $Z_{L,\mathrm{opt}} = 12 + j10\ \Omega$ and $Z_{L,\mathrm{opt}} = 17 + j22\ \Omega$, respectively. For $6 \times 50\ \mu$m, the optimum $Z_{L,\mathrm{opt}}$ is low and make narrowband matching a certainty. Stacking transistors for generating higher output power in GaAs and other related low-bandgap materials have, therefore, a great benefit of their higher $Z_{L,\mathrm{opt}}$ impedance.

C. Stacked HEMT Modeling

The stacked HEMT, including the breakouts of the CS HEMT, and the second HEMT were laid out according to the foundry design rules. The scalable transistor model used in the design was developed in-house and used in the design of the PA [7]. The following measurements were performed to extract the large signal model: scattering parameters (SPs), IV, and power spectrum. To evaluate and verify the quality of the model, additional active load pull was made using a large signal vector network analyzer (LSNA) setup at the Chalmers University of Technology [8]. The LSNA setup is capable of measuring harmonics up to 50 GHz. To be able to capture the waveform accurately, a minimum of three harmonics is usually necessary. Ideally, the stacked HEMT is not frequency dependent, since voltage division occurs between C_{GS2} and C_{a1}, and therefore, LSNA measurement could be performed at an input fundamental frequency of 10 GHz while monitoring up to five harmonics. However, the presence of a gate inductance will make the voltage division frequency dependent, and therefore make the concept frequency limited. The maximum frequency of operation is discussed in Section II-D. Even though the stacked HEMT and the design were optimized at 60 GHz, the LSNA measurement verifies the enhanced output power and voltage swing that theoretically should double (at low frequency) if C_{a1} is optimally selected for power. The LSNA measurements also verify the higher optimum power load impedance ($Z_{L,\mathrm{opt}}$) and gain. In Figs. 4 and 5, the CS HEMT of 300 μm and a stacked HEMT of 600 μm are compared for output power and power added efficiency (PAE), while actively changing the load impedance using the LSNA setup. The load impedance chart of the stacked HEMT is swept with a radius of 0.6 with origin at $\Gamma = 0$ and an angle between 0° and 90° and the CS HEMT with a radius of 0.5 and an angle between 90° and 180°. Both the higher output power and the higher $Z_{L,\mathrm{opt}}$ are clearly visible in Figs. 4 and 5.

In Fig. 6, the gain and efficiency are plotted versus output power at the optimum load impedance for the CS HEMT and the stacked HEMT at 10 GHz. The small-signal gain and the saturated output power are close to 3 dB higher, the theoretical optimum. The stacked HEMT shows enhanced output power, delivering a maximum output power of 25.5 dBm, biased at 8 V and 75 mA in comparison with 22.7 dBm at 4 V and 75 mA for the CS HEMT (both at current density of 0.25 A/mm). The efficiency dropped negligibly from

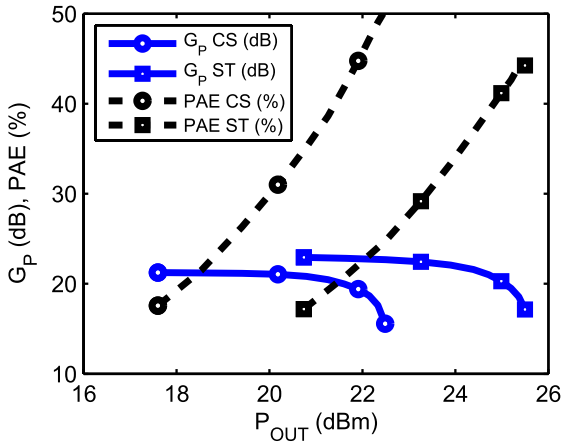

Fig. 6. Measured power gain (blue continuous line) and PAE (dashed black line) versus output power at optimum load impedance of the stacked HEMT (squares) and the CS HEMT (circles) at 10 GHz.

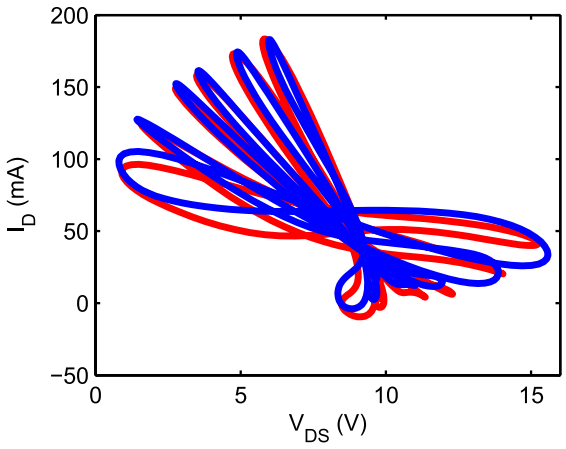

Fig. 7. Measured and simulated waveforms while varying the load impedance of the stacked HEMT between 5 and 500 Ω. Blue traces are the simulated waveforms and red traces are measurements.

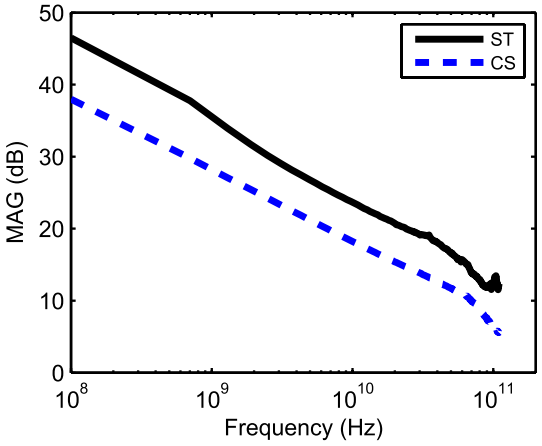

Fig. 8. Calculated MAG from the measured SP up to 110 GHz for the stacked HEMT (black solid line) and the CS HEMT (blue dashed line).

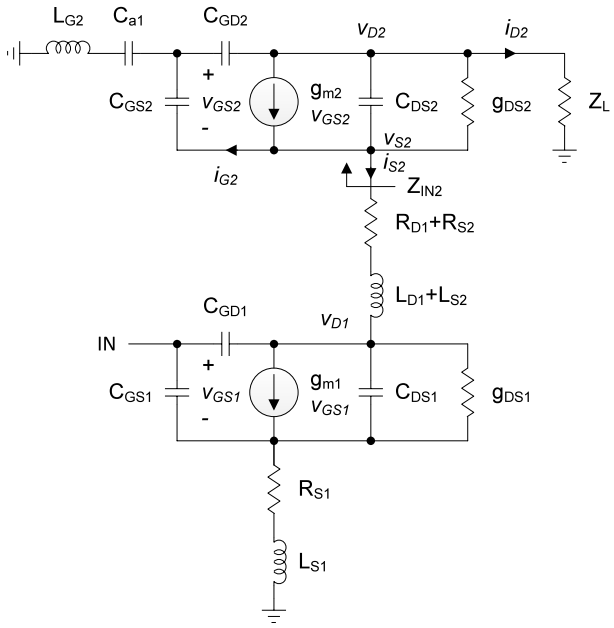

Fig. 9. Schematic of the small-signal model for the stacked HEMT.

49% to 44% at maximum output power. In power combining networks, especially at mm-wave frequencies, losses are always present which will lower the efficiency.

In Fig. 7, the stacked HEMT model was compared with LSNA measurements varying the load impedance between 5 and 500 Ω. The evaluation confirms the fit between model and measurement, in particular, in the important knee and breakdown regions.

In Fig. 8, the maximum available gain (MAG) is calculated from the SP measurements up to 110 GHz on the CS HEMT and the stacked HEMT. Similar to the cascode, the stacked HEMT delivers improved high-frequency performance. In addition to the enhanced high-frequency performance, the stacked HEMT also delivers higher output power and optimum output power impedance. The stacked HEMT provides one extra degree of freedom in selecting the transistor size that is optimum for power, gain, and output impedance. Furthermore, the stacked HEMT allows the use of larger devices at higher frequencies.

D. Stacked HEMT Stability and Analysis

Cascode HEMTs have a reputation of being difficult to stabilize, as does the stacked HEMT due to its similar configuration. The main problem with this configuration is the negative input impedance that occurs at high frequencies at the source of the second HEMT when there is an inductance to ground at the gate terminal. In this particular process, the inductance per via is estimated to be 18 pH, plus 20 pH that arises from the gate finger inductance and gate access lines. In this section, the input impedance at the source of the second HEMT will be analytically analyzed with respect to the gate inductance (L_{G2}) and external capacitance (C_{a1}) and illustrates the effect with simulations. Finally, the used transistor layout in the design for high-frequency operation will be described.

The input impedance of the second HEMT (Z_{IN2}) in Fig. 9 is calculated from (4) to (6) under the simplification of

neglecting C_{GD2} for the purpose of finding an approximate expression for Z_{IN2}. In (7), specifically, the first term is the major contributor to the real part of Z_{IN2} and has a pole at $\omega_{neg} = ((C_{a1} + C_{GS2})/(L_{G2}C_{a1}C_{GS2}))^{1/2}$. It is a combination of C_{a1}, C_{GS2}, and L_{G2} and increases with lower L_{G2} and lower C_{a1}. Beyond this frequency point, the real part of Z_{IN2} becomes negative. The parameters should (if possible) be selected such that the pole occurs above f_{max} of the device to avoid instabilities

$$Z_{IN2} = -\frac{v_{S2}}{i_{S2}} = \frac{v_{S2}}{i_{G2} + i_{D2}} \tag{4}$$

where

$$i_{G2} = v_{S2}(1/j\omega C_{GS2} + 1/j\omega C_{a1} + j\omega L_{G2})^{-1} \tag{5}$$

$$i_{D2} = v_{S2}\left(\frac{j\omega L_{G2} + 1/j\omega C_{a1}}{1/j\omega C_{GS2} + 1/j\omega C_{a1} + j\omega L_{G2}} - 1\right) g_{m2} + v_{S2}((j\omega C_{DS2} + g_{DS2}) \parallel Y_L) \tag{6}$$

so that

$$Z_{IN2} = \left(g_{m2}\frac{C_{a1}}{C_{A1} + C_{GS2} - \omega_{neg}^2 L_{G2}C_{a1}C_{GS2}} + Y_L\frac{j\omega C_{DS2} + g_{DS2}}{j\omega C_{DS2} + g_{DS2} + Y_L} + \frac{j\omega C_{a1}C_{GS2}}{C_{a1} + C_{GS2} - \omega^2 L_{G2}C_{a1}C_{GS2}}\right)^{-1}. \tag{7}$$

To address the measure of stability for the device configuration, the stability factor k is used and calculated using (8). To be stable, k must be larger than 1, as stated in (8). The first term of the nominator carries the real part of the input admittance; hence, the stability factor strongly depends on L_{G2} and C_{a1}. This negative impedance does not necessarily translate to an unstable device, but rather a possible source of instability and a negative contributor to the stability factor

$$k = \frac{\Re(Y_{11})\Re(Y_{22}) - \Re(Y_{12}Y_{21})}{|Y_{12}Y_{21}|} > 1. \tag{8}$$

In comparison to a true cascode cell, where the gate should be RF grounded, the second HEMT shall divide the voltage between the intrinsic C_{GS} and extrinsic C_{a1} to make $|v_{DS1}|$ and $|v_{DS2}|$ equal. To fulfill this condition, the external capacitance C_{a1} results in a fairly low value and as a consequence, the series resonance with C_{GS2}, C_{a1}, and L_{G2} occurs at a higher frequency than that of the cascode, and therefore contributing to improving stability. Fig. 10 shows the simulated real part of Z_{IN2} versus C_{a1}. Two effects arise, the series resonance frequency of C_{a1}, C_{GS2}, and L_{G2} as well as the increased input impedance with decreased C_{a1}, improving the high frequency stability.

The input impedance Z_{IN2} of the second HEMT is also very important from a power perspective, because it determines the load impedance of the CS. Consequently, $\Re(Z_{IN2})$ depends on C_{a1}, which is shown in Fig. 10. Since the common-gate configuration has a current gain $\leq$1, the stacked HEMT's current swing depends solely on the CS HEMT. Furthermore, since the voltage swings across the drain–source terminals of the two transistors add constructively, both the voltage and current swings from the CS HEMT must be maximized to deliver the maximum output power. Therefore, the CS HEMT needs to be power matched.

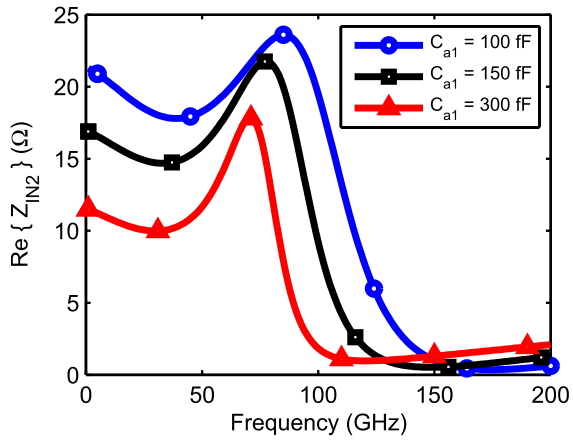

Fig. 10. Simulated real part of Z_{IN2} versus frequency at three capacitance values of C_{a1}: 100 fF (blue line with circles), 150 fF (black line with squares), and 300 fF (red line with triangles). The number of vias in the simulation is 4.

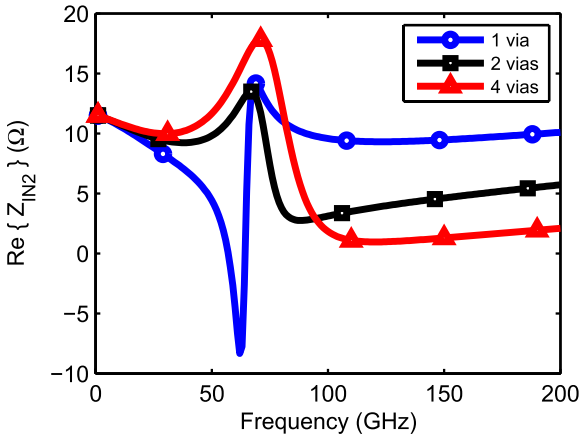

Fig. 11. Simulated real part of Z_{IN2} versus frequency for n number of vias on the gate terminal of the second HEMT: 1 via (blue line with circles), 2 vias (black line with squares), and 4 vias (red line with triangles). All are simulated with $C_{a1} = 300$ fF.

Fig. 11 shows the simulated real part of Z_{IN2} versus n number of vias on the gate terminal of the second HEMT. A low gate inductance is important since it otherwise can give rise to a negative input impedance when C_{a1} and L_{G2} are too high, see the negative input impedance at 60 GHz in Fig. 11. The reduced gate inductance not only improves the stability of the transistor with frequency, but also increases the maximum operating frequency of which the input impedance to the second HEMT is the optimum load impedance of the CS HEMT.

The stability factor is directly related to the two parameters L_{G2} and C_{a1} and results in a less stable configuration when either one of the two parameters increase. In Fig. 12, the stability factor is plotted for three different number of vias, with C_{a1} fixed at 150 fF. The positive effect of a lower gate inductance for the stability factor is evident.

The transistor layout plays a major role when trying to lower the gate inductance and thereby increase the stability factor

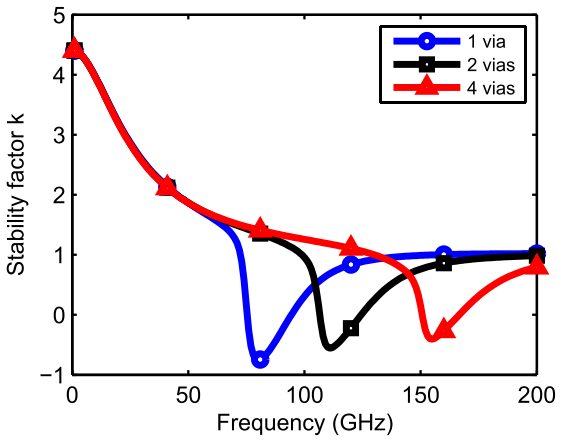

Fig. 12. Simulated stability factor k versus frequency for n number of vias on the gate terminal of the second HEMT: 1 via (blue line with circles), 2 vias (black line with squares), and 4 vias (red line with triangles). All are simulated with $C_{a1} = 150$ fF.

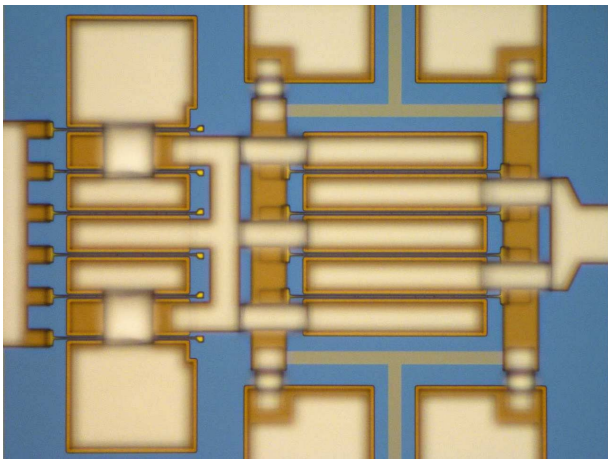

Fig. 13. Layout of the stacked HEMT cell, showing the 6×50 μm CS HEMT to the left and 4×75 μm second HEMT with four gate vias to the right.

at high frequencies. Fig. 13 shows the configuration of the stacked HEMT, where three main implementations were used to lower the gate inductance of the second HEMT. Both the CS HEMT and the second HEMT have 300-μm total gate width, distributed with 6- and 50-μm wide fingers for the CS HEMT and 4- and 75-μm wide fingers for the second HEMT. First, the change from 6 to 4 gate fingers for the second HEMT reduces the physical length from the intrinsic gate to the ground vias, further reducing the excess gate inductance. Second, the four gate fingers were anchored on both sides and finally, four ground vias were connected to the gates. All these implementations contribute to higher frequency operation of the stacked HEMT.

III. Results

The circuit has been verified on wafer with two-port SPs up to 67 GHz and characterized with one- and two-tone power measurements, quantified in terms of $P_{1\text{dB}}$, P_{SAT} (1- and 4-dB output referred compression points), and third-order intermodulation products (OIP3). The stacked HEMT amplifier is characterized with a current density of 0.25 A/mm, $V_{D1} = 3.3$ V, and $V_{D2} = 6$ V. The gate voltage for this current density is approximately $V_{G1,G2} = -0.45$ V. In the simulations, we were only able to set the ambient temperature, but since the stacked HEMT interact thermally (see Fig. 18), the channel temperature is higher in that particular device and as a result, the measured performance is lower. Furthermore, the transistor model did not include the temperature dependence of critical parameters, such as R_S and R_D, which will contribute to optimistic simulation results. To achieve better agreement between simulations and measurements, a more advanced stacked HEMT transistor model with enhanced temperature-dependent parameters and circuit thermal coupling must be iterated to gain accuracy in the prediction between simulations and measurements.

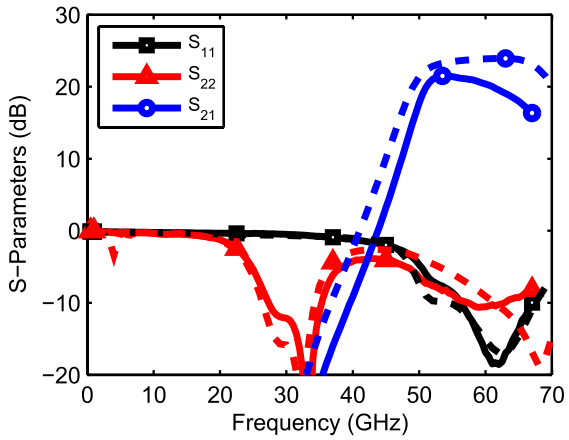

Fig. 14. Measured (continuous line) and simulated (dashed line) SP between 0 and 67 GHz.

A. S-Parameters

The vector network analyzer used in the measurements was a 67-GHz Agilent E8361A. The probes were Picoprobe 67A together with corresponding calibration substrate #CS-5 and LRM calibration method. Fig. 14 shows the frequency response from the SP measurements. The gain and the return loss measure the flat response of 22 dB and low return loss better than 10 dB within the 60-GHz ISM band.

B. Output Power and Efficiency

The output power and efficiency were measured with an Agilent 83623B signal generator together with a six times frequency multiplier and electronically controlled attenuator to adjust the power level. An Agilent E4407B spectrum analyzer and an Agilent 11974V harmonic mixer with 40-dB attenuator were used to measure the output power from the PA. The gain, output power, and PAE are plotted in Fig. 15 and show maximum PAE of 15% and 25-dBm saturated output power. The saturated output power and 1-dB gain compression are plotted versus frequency in Fig. 16.

C. Linearity

Two-tone measurement was performed with a similar setup as described in Section III-B with an extra six times multiplier and a 3-dB WR15 hybrid from Aerowave Ltd. to form the two-tone source. The OIP3 of the harmonic mixer and attenuator

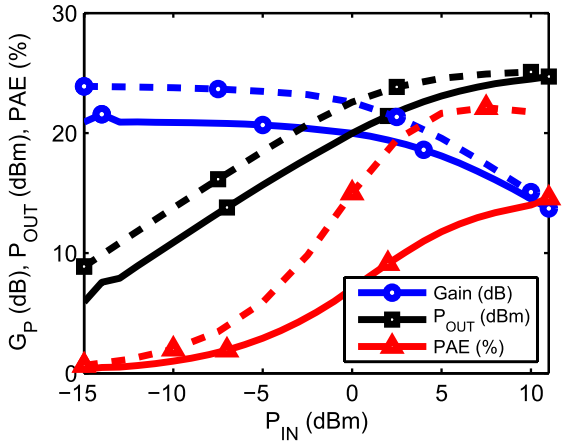

Fig. 15. Measured (continuous line) and simulated (dashed line) output power (black lines with squares), gain (blue lines with circles), and efficiency (red lines with triangles) of the stacked HEMT PA at 61 GHz versus input power.

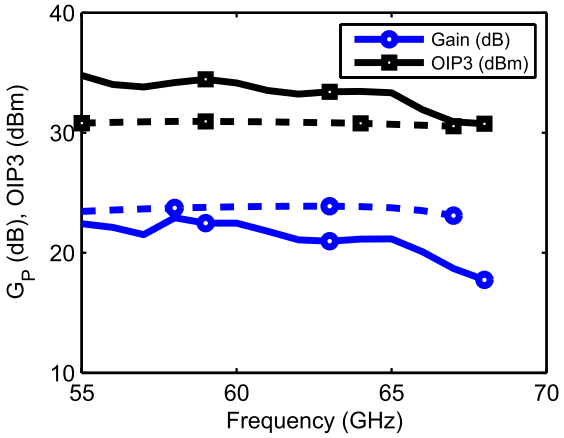

Fig. 17. Measured (continuous line) and simulated (dashed line) OIP3 (black lines with squares) and gain (blue lines with circles) versus frequency with −10-dBm input power.

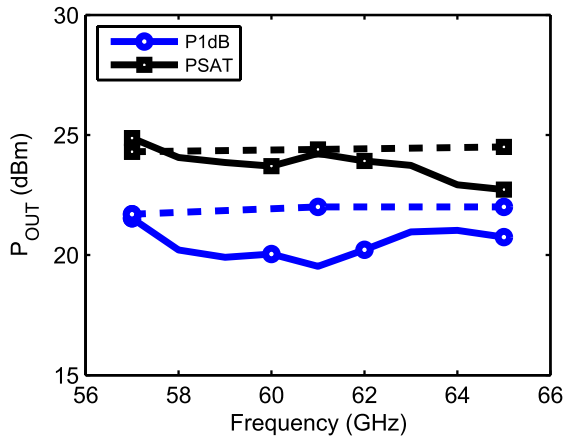

Fig. 16. Measured (continuous line) and simulated (dashed line) P_{1dB} (blue lines with circles) and P_{SAT} (black lines with squares) versus frequency.

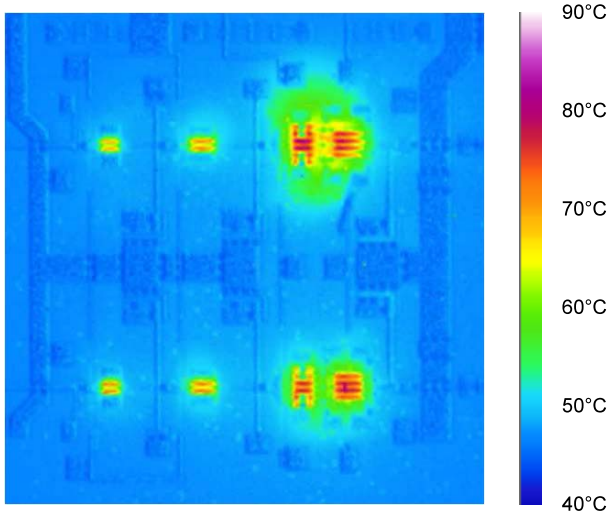

Fig. 18. Measured infrared image at nominal bias with input signals off. The base plate reference temperature is set at 45 °C.

was estimated to be 40 dBm, giving enough headroom to ensure that the intermodulation products generated by the harmonic mixer will not be measured. In Fig. 17, the OIP3 and gain are plotted versus frequency, where the maximum OIP3 was measured to 34 dBm at 59 GHz.

D. Thermal Mapping

The PA was measured with an infrared microscope from Quantum Focus Instruments to thermally map the chip. The output power transistors have a total periphery of 1.2 mm, each dissipating around 500-mW dc power. Since GaAs has poor thermal conductivity (0.55 W/cm K), it is important to verify the channel junction temperature of the devices, such that they operate at temperatures that do not overheat or damage the transistors. In Fig. 18, the chip is biased at nominal bias with no input signal. The larger devices interact thermally with each other, resulting in a channel junction temperature of 38 °C above ambient temperature at 6 V operation, slightly higher than the driver stages and increasing to 47 °C above ambient temperature when the drain voltage is 7 V. The thermal resistance for the chip is calculated to 29.6 °C/W.

E. Comparison

In Table II, mm-wave PAs utilizing stacked transistors [3], [5], [9] (single or multiple transistor(s) cascaded to a CS transistor) in SOI, BiCMOS, and GaAs technologies are compared. In addition to the stacked topology in the comparison, [10]–[13] report the highest output power from a mm-wave MMIC in GaAs, InP, and Cascode GaN, respectively. This mm-wave PA with an operating voltage of 6 V and 25-dBm saturated output power at 61 GHz reports, to the best of our knowledge, the highest output power of stacked transistors in the open literature. In addition, its compact size contributes to make this PA the most power dense GaAs mm-wave MMIC ever reported with a power density (P_{SAT}/chip area) of 100 mW/mm^2, demonstrating the possibilities of the stacked technology in GaAs. Although the stacked HEMT concept has many positive features, the imperfect voltage addition from the CS HEMT and the second HEMT limits the use of the stacked HEMT for efficient power combining at frequencies close to f_T of the process, because of the time delay in the

TABLE II
COMPARISON OF PAs PUBLISHED IN THE OPEN LITERATURE

	[10]	[5]	[9]	[13]	[3]	[11]	[12]	This work
Frequency (GHz)	71-76	56-62	38-42	56-65	47.5	62.5	59-64	55-64
Gain (dB)	na	15	15	22	12.8	13	15	22
P_{1dB} (dBm)	27	19	na	22.5	16	25.5	28	22
P_{SAT} (dBm)	29	20.0	22	24.8	20.3	27.5	30	25
PAE (%)	15	19	21	8	19.4	21	21	15
Power density ($\mathrm{mW/mm^2}$)	88	18	158	151	134	54	na	100
Size ($\mathrm{mm^2}$)	9	5.7	1.0	2.0	0.8	10.4	na	3.2
Technology	GaAs	GaAs	SiGe	GaN	SOI	GaAs	InP	GaAs
f_T/f_{max} (GHz)	135/200	na	200/280	na	250/180	na	120/na	135/200

second HEMT. Thermal improvements in the circuit design will help to contribute to a higher PAE, as predicted in the simulations. Therefore, the PAE is moderate in comparison with other designs in Table II but due to the compact power combining technique, the power density becomes higher.

IV. CONCLUSION

A stacked HEMT mm-wave PA with high output power and power density, implemented in a commercial 0.1-μm InGaAs pHEMT technology has been demonstrated. The stability problem of the stacked HEMT has been analyzed and an alternative layout with improved stability and high-frequency characteristics has been presented. The stacked HEMT PA is based on this layout. The stacked concept has previously been evaluated in, for instance, CMOS with improved output power capability. This three-stage PA reports the highest output power at mm-wave frequencies of all stacked FET designs in all technologies and measures 15% PAE and 25-dBm saturated output power. Furthermore, it reports the highest power per $\mathrm{mm^2}$ *V*-band amplifier in GaAs.

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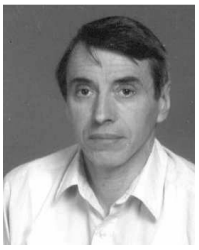

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