

## 7 FEATURES

- 26/28 dBm P1dB/PSAT
- E1-band coverage
- 34 dBm OIP3
- 21 dB gain
- Integrated PD & ED detectors

## TYPICAL APPLICATIONS

- Point-to-point communication
- Instrumentation
- Fiber over radio
- 77 GHz automotive radar

## DESCRIPTION

gAPZ0051 is a power amplifier in the 71-76 GHz frequency band suitable for E-band point-to-point communication and 77 GHz automotive radar. Integrated on chip are a high dynamic range output power detector, a wide band envelope detector and a temperature sensor. The PA utilizes multiple parallel transistors to increase efficiency and output power. The PA has high linearity, high efficiency, low input/output return loss and flat gain response.

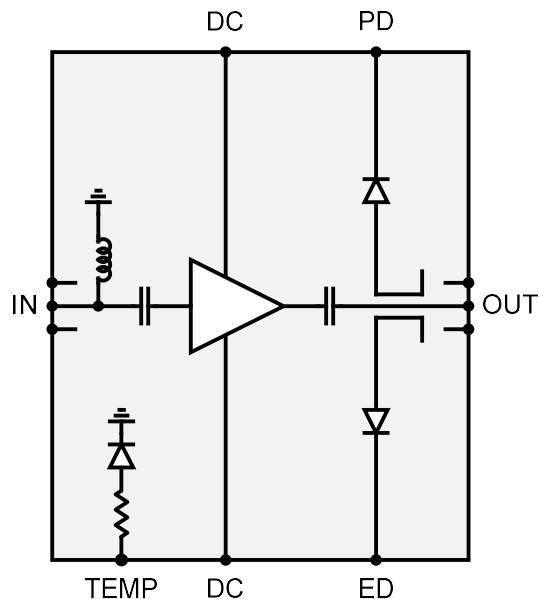


Figure 1. Block diagram of the PA.

## ELECTRICAL PERFORMANCE

Table 1. Electrical performance  $T_A=25^\circ\text{C}$ 

Parameter	Min	Typ	Max	Unit
Frequency	71 (68)		76 (79)	GHz
Gain		21		dB
Gain ripple				dB/GHz
P1dB		26		dBm
PSAT		28		dBm
OIP3		34		dBm
PAE			25	%
NF		6		dB
Input return loss	6			dB
Output return loss	7			dB
Power consumption		2200		mW

## MEASURED PERFORMANCE

The chip has been measured on-wafer using CW and 2-tone input test signals. The PA uses typical bias settings if not specified differently.

Table 2. Test conditions

Parameter	Setting
RF input power	-10 dBm/tone
RF input frequency	73.5 GHz
Frequency separation	10 MHz
Temperature	+25°C

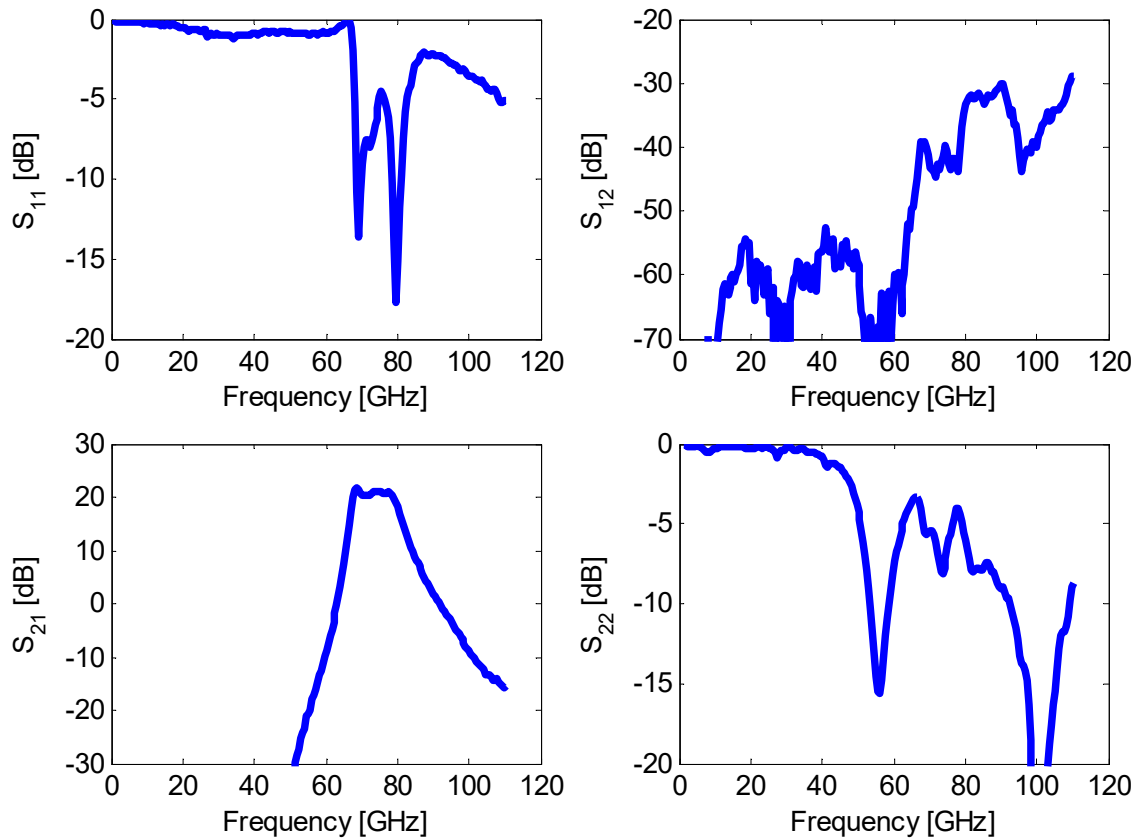
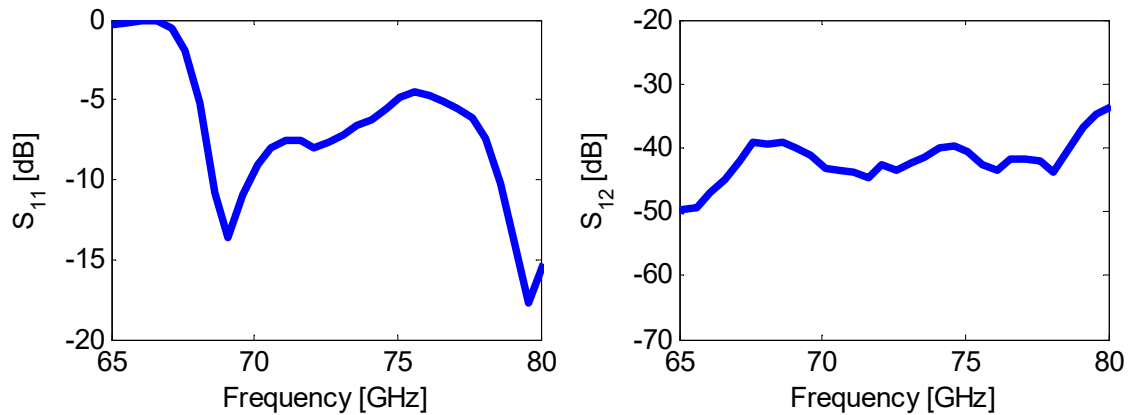


Figure 2. Small signal response from 0-120 GHz at nominal bias. (Upper left): Input return loss. (Upper right): Reverse isolation. (Lower left): Small-signal gain. (Lower right): Output return loss.



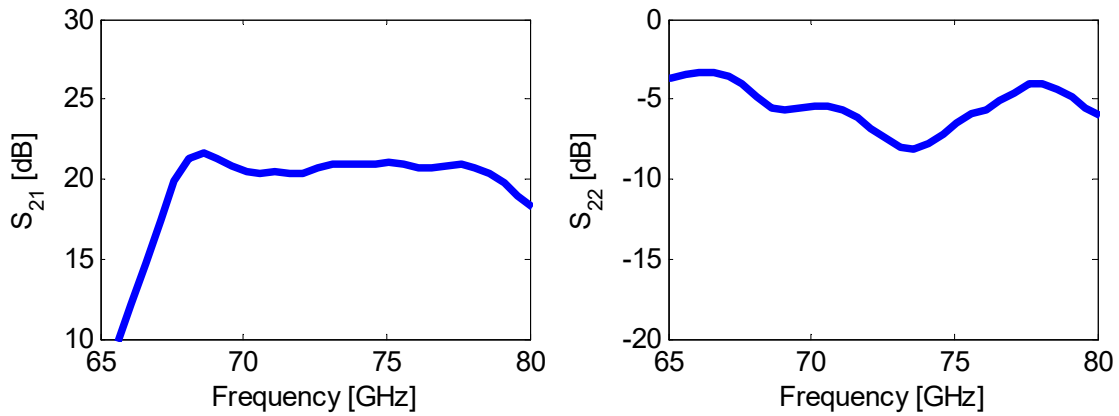


Figure 3. Small signal response within the E1-band at nominal bias. (Upper left): Input matching. (Upper right): Reverse isolation. (Lower left): Small-signal gain. (Lower right): Output return loss.

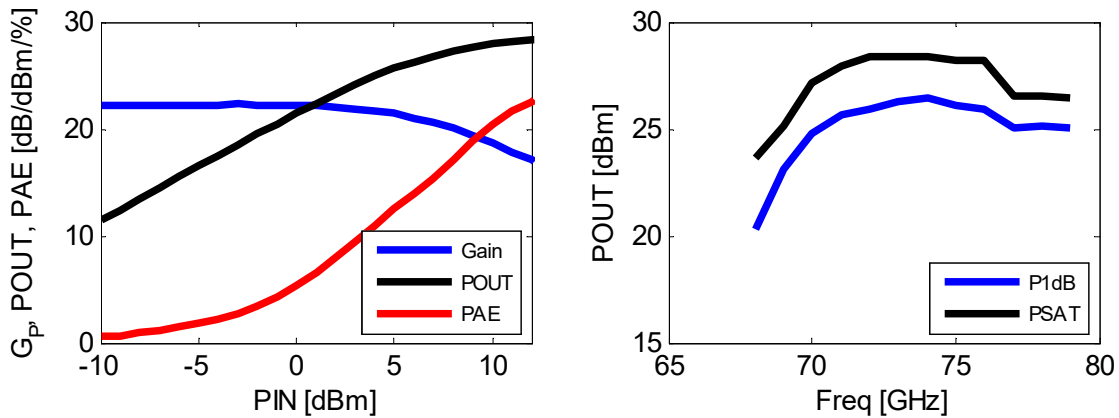


Figure 4. (Left): Output power, gain and PAE vs input power at 73 GHz. (Right): P1dB and PSAT vs freq.

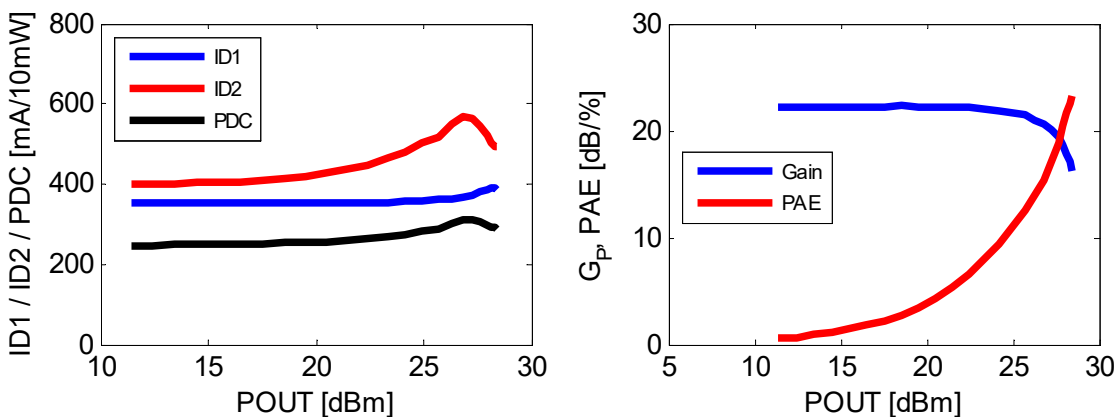


Figure 5. (Left): Power dissipation and drain currents ID1 and ID2 vs output power at 73 GHz. (Right): Efficiency vs output power at 73 GHz.

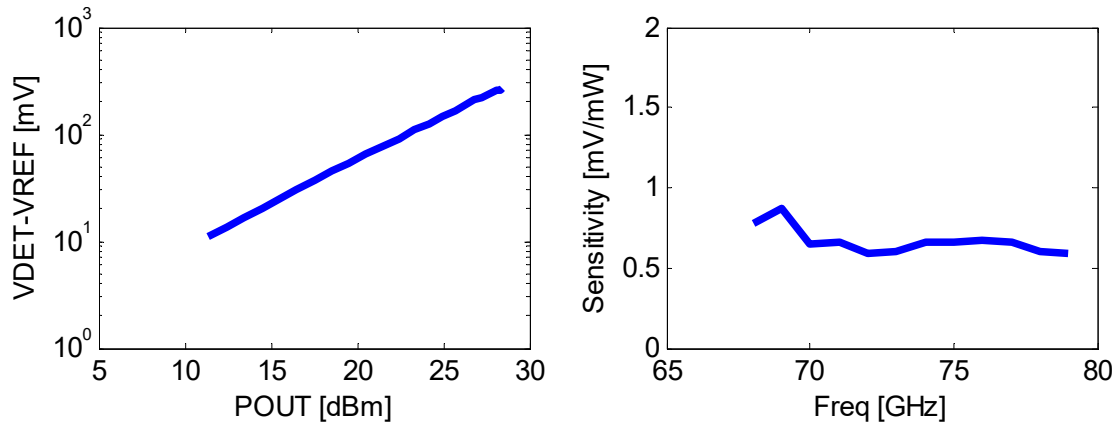


Figure 6. (Left): Power detector output voltage vs output power at 73 GHz and 1 G $\Omega$  load impedance. (Right): Power detector voltage sensitivity vs frequency at 20 dBm output power and 1 G $\Omega$  load impedance.

## RECOMMENDED OPERATING CONDITIONS

Bias should first be applied to the gates (VG...) followed by the drains (VD...). The gate voltages must be adjusted within the min/max range indicated in Table 3-5 to obtain the specified drain currents. The drain currents are stated with on input signal.

Table 3. Electrical settings on connector P1

Connector P1	Pad No.	Bias settings (V/mA)			I/O
		Min	Typ	Max	
NC	1				NC
VD1_PA <sup>[1]</sup>	2	3.2	3.3 / 275	3.4	Input
VG1_PA <sup>[1]</sup>	3	-0.7	-0.5	-0.3	Input
VG2_PA <sup>[1]</sup>	4	-0.7	-0.5	-0.3	Input
GND	5				Ground
VD2_PA <sup>[1]</sup>	6	3.2	3.3 / 400	3.4	Input
VG_PD <sup>[2]</sup>	7	0.6	0.8	1.0	Input
VREF_PD	8	0	0.2		Output
VOUT_PD	9	0		2	Output

Table 4. Electrical settings on connector P2

Connector P2	Pad No.	Interface	I/O
GND	10		Ground
RF_OUT	11	Z <sub>0</sub> = 50 Ohm, AC coupled	Output
GND	12		Ground

Table 5. Electrical settings on connector P3

Connector P3	Pad No.	Bias settings (V/mA)			I/O
		Min	Typ	Max	
VOUT_ED	13				Output
VD_ED	14	3.2	3.3	3.4	Input

<sup>1</sup> VG1, VG2, VD1 and VD2 are physically connected across the chip via P1 and P3. Both connectors must be biased for maximum performance. Total current for connectors P1 and P3 is specified.

<sup>[2]</sup> Maximum sensitivity is achieved at threshold voltage.

VG_ED <sup>[2]</sup>	15	-1.0	-0.8	-0.6	Input
VD2_PA <sup>[1]</sup>	16	3.2	3.3 / 400	3.4	Input
GND	17				Ground
VG2_PA <sup>[1]</sup>	18	-0.7	-0.5	-0.2	Input
VG1_PA <sup>[1]</sup>	19	-0.7	-0.5	-0.2	Input
VD1_PA <sup>[1]</sup>	20	3.2	3.3 / 275	3.4	Input
VG_TEMP	21	3.2	3.3 / 1	3.4	I/O

Table 6. Electrical settings on connector P4

Connector P4	Pad No.	Interface	Function
GND	22		Ground
RF_IN	23	Z <sub>0</sub> = 50 Ohm, AC coupled	Input
GND	24		Ground

## **ABSOLUTE MAXIMUM RATINGS**

Table 7. Absolute maximum ratings

Gate-source voltage	-2 to +0.7 V
Drain-source voltage	4.5 V
Gate-drain breakdown voltage	8 V
ID1, ID2	720 mA
RF input power	+20 dBm
Operating temperature	-40 to + 85°C
Storage temperature	-65 to +150°C



## OUTLINE DRAWING

Mechanical drawing with pad locations is also available in dxf-file format on the web. The substrate thickness is 50  $\mu\text{m}$  (GaAs).

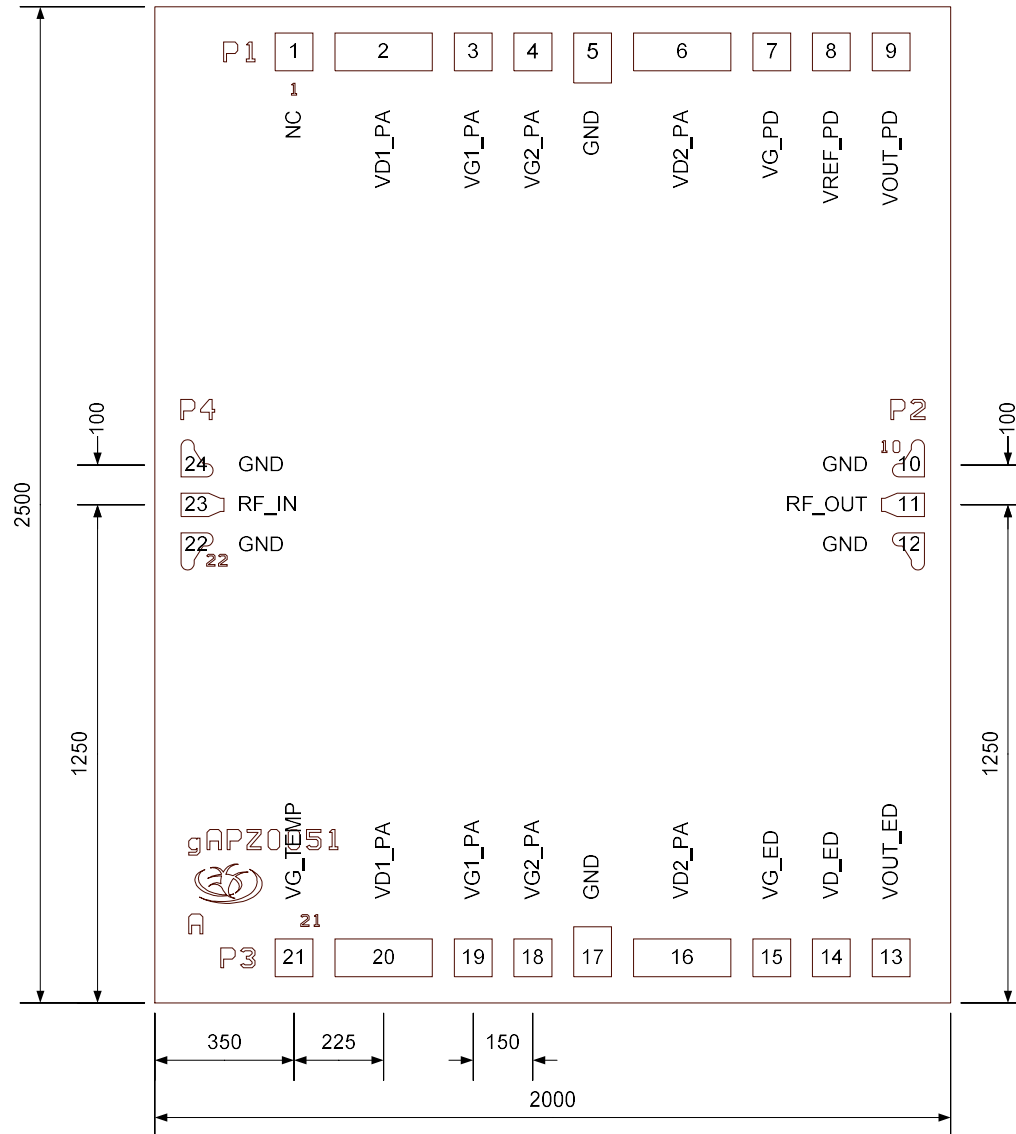


Figure 7. Outline drawing of the MMIC. Dimensions are in  $\mu\text{m}$ .