gAPZ0079B
V-band Power Amplifier
57-71 GHz (56-72 GHz)

Features

- 57-71 GHz
- 27/28 dBm P1dB/PSAT
- 37 dBm OIP3
- 15 dB gain
- Integrated detectors
- Nominal bias: 4.0 V and 1.2 A
- Size: 4 x 2.5 x 0.05 mm

Applications

- Point-to-point communication
- Radar and imaging
- Instrumentation
- Fiber over radio

Description

The gAPZ0079B is a bare die GaAs pHEMT three-stage power amplifier MMIC optimized for 57-71 GHz. It has 15 dB gain and 37 dBm OIP3 making it ideal for long-range spectral efficient V-band point-to-point communication.

At a nominal bias of 4.0 V and 1.2 A the MMIC dissipates 4.8 W and deliver 28 dBm saturated power at 10 % PAE.

Two temperature compensated detectors are integrated on-chip and can be configured for RMS power or envelope detection.

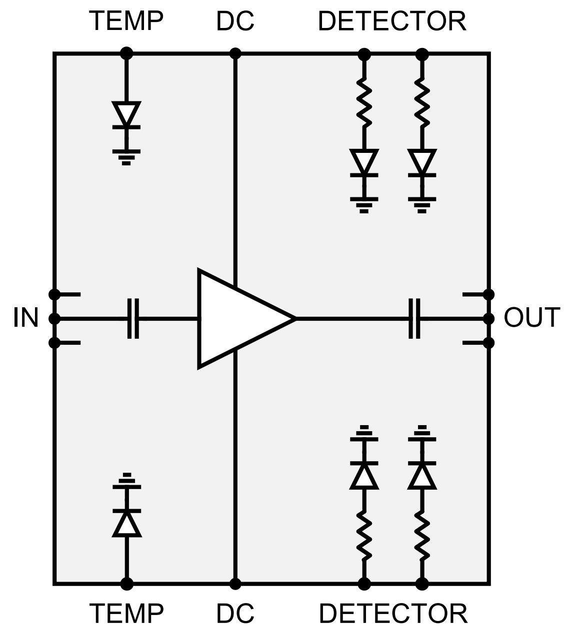


Figure 1. Circuit block diagram

Data and specification are subject to change without notice © 2020 Gotmic AB
Gotmic AB, Arvid Hedvalls Backe 4, S-411 33 Göteborg, Sweden. Tel: +46 (0) 31 184 030
www.gotmic.se/

ELECTRICAL SPECIFICATIONS

Table 1. Electrical specifications, backside temperature +25 °C, nominal bias

Parameter		Min	Typ	Max	Unit
Frequency Range (performance)		57		71	GHz
Frequency Range (extended)		56		72	GHz
Gain			15		dB
Gain Temperature Slope			-0.05		dB/°C
OP1dB			27		dBm
PSAT (3 dB compression)			28		dBm
PAE at PSAT			10		%
OIP3			37		dBm
Input Return Loss			15		dB
Output Return Loss			15		dB
Detector Output at POUT *(VREF - VDET)*	-10 dBm		3		mV
	0 dBm		20		
	10 dBm		100		
	20 dBm		500		
	30 dBm		2000		
PDC (quiescent)	3.3 V / 1.2 A		3960		mW
	4.0 V / 1.2 A		4800		

Table 2. Absolute maximum ratings

Parameter	Rating
Gate voltage (VG..)	-2.0 V
Drain voltage (VD..)	+4.5 V
Drain currents:	
ID1_A + ID1_B	280 mA
ID2_A + ID2_B	540 mA
ID3_A + ID3_B	800 mA
DET_A, DET_B, REF_A and REF_B	1 mA
TEMP_A and TEMP_B	1 mA
RF input power	+23 dBm
Junction temperature (1 million hours MTTF)	+150 °C
Thermal resistance (+85 °C backside temp, incl. epoxy)	*9 °C/W*
Operating temperature	-40 to +85 °C
Storage temperature	-65 to +150 °C

Data and specification are subject to change without notice © 2020 Gotmic AB

Pad Configuration and Bias

Always apply the gate supplies first followed by the drain supplies. It is recommended to initially set all gates to -1.6 V and adjust the gate supplies to obtain the specified drain currents.

The typical gate voltage can vary by up to 0.2 V from what is noted. The drain currents are listed with all RF input signals off.

When gates and drains are combined external to the chip using a common gate and drain supply, adjust the common gate voltage to achieve a total drain current of 1.2 A.

Table 3. Pad configuration on connector P1

Pad No.	Reference	Supply (V)	Current (mA)	Function
1	TEMP_A	See temperature sensor		Temperature output
2	VG1_A	-0.5 (typ.)		Bias
3	VD1_A	4.0	100	Bias
4	VG2_A	-0.5 (typ.)		Bias
5	VD2_A	4.0	200	Bias
6	GND			GND
7	VG3_A	-0.5 (typ.)		Bias
8	VD3_A	4.0	300	Bias
9	VREF_A	See detector operation		Detector reference
10	VDET_A			Detector output

Table 4. Pad configuration on connector P2

Pad No.	Reference	Interface	Function
11	GND		GND
12	RF_OUT	50 Ohm, open-circuit at DC	RF output
13	GND		GND

Data and specification are subject to change without notice © 2020 Gotmic AB

Table 5. Pad configuration on connector P3

Pad No.	Reference	Supply (V)	Current (mA)	Function
14	VDET_B	See detector operation		Detector output
15	VREF_B			Detector reference
16	VD3_B	4.0	300	Bias
17	VG3_B	-0.5 (typ.)		Bias
18	GND			GND
19	VD2_B	4.0	200	Bias
20	VG2_B	-0.5 (typ.)		Bias
21	VD1_B	4.0	100	Bias
22	VG1_B	-0.5 (typ.)		Bias
23	TEMP_B	See temperature sensor		Temperature output

Table 6. Pad configuration on connector P4

Pad No.	Reference	Interface	Function
24	GND		GND
25	RF_IN	50 Ohm, open-circuit at DC	RF input
26	GND		GND

Data and specification are subject to change without notice © 2020 Gotmic AB

TYPICAL PERFORMANCE

Unless otherwise noted, all data presented has been obtained from on-wafer measurements, at room temperature and at nominal bias.

The two-tone RF input signal at -10 dBm/tone has a separation frequency of 50 MHz.

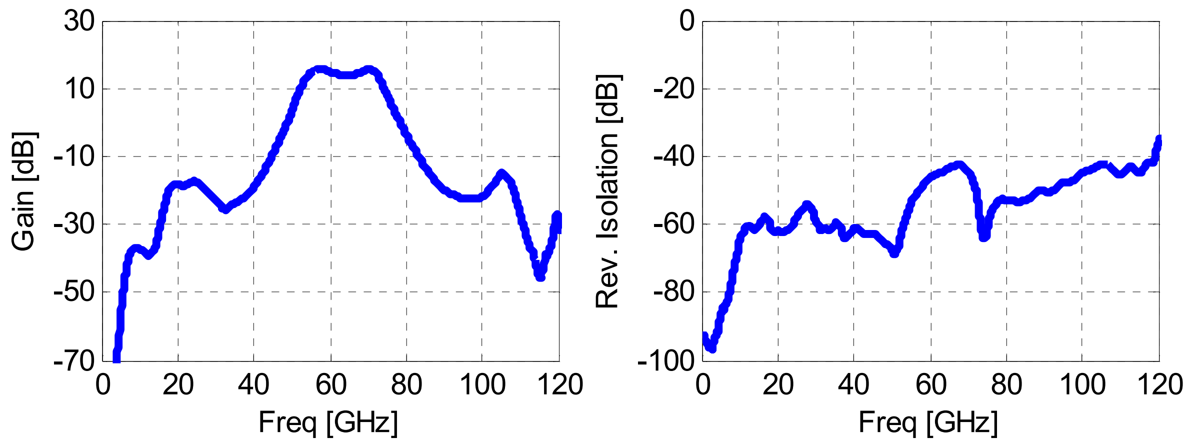


Figure 2. Gain (left) and reverse isolation (right)

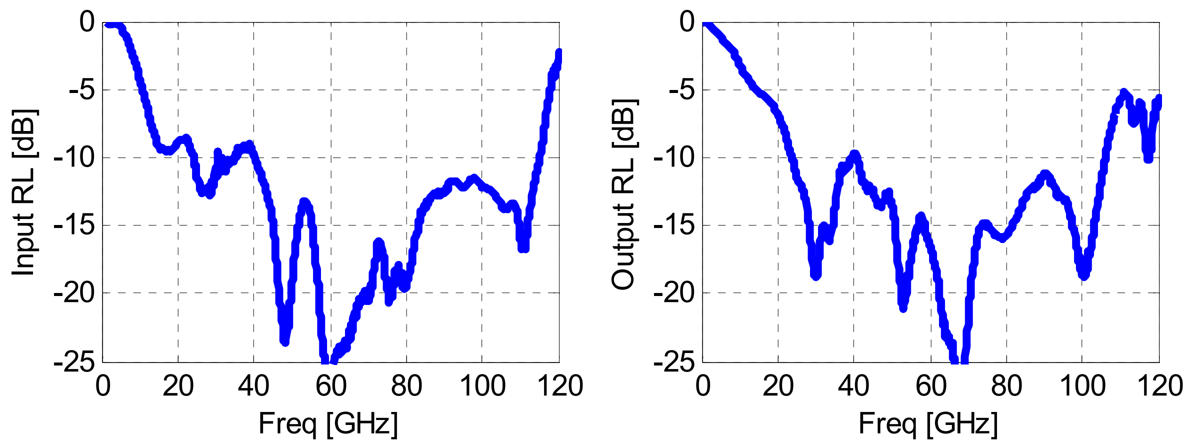


Figure 3. Input (left) and output return loss (right)

Data and specification are subject to change without notice © 2020 Gotmic AB
Gotmic AB, Arvid Hedvalls Backe 4, S-411 33 Göteborg, Sweden. Tel: +46 (0) 31 184 030
www.gotmic.se/

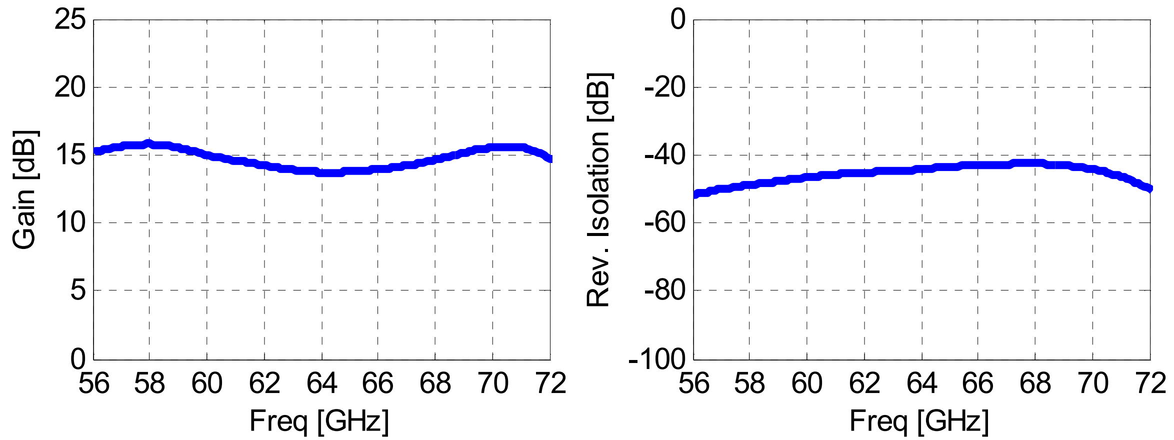


Figure 4. In-band gain (left) and reverse isolation (right)

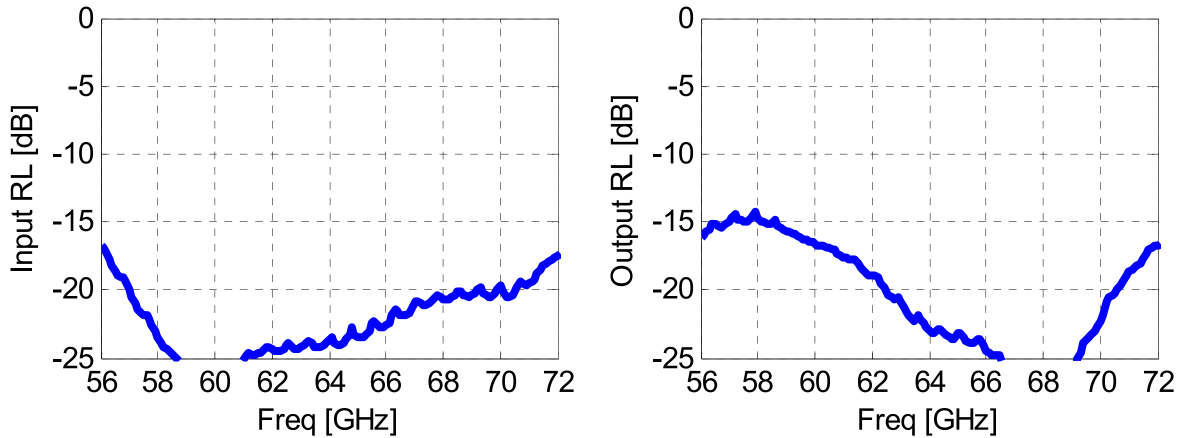


Figure 5. In-band input (left) and output return loss (right)

Data and specification are subject to change without notice © 2020 Gotmic AB

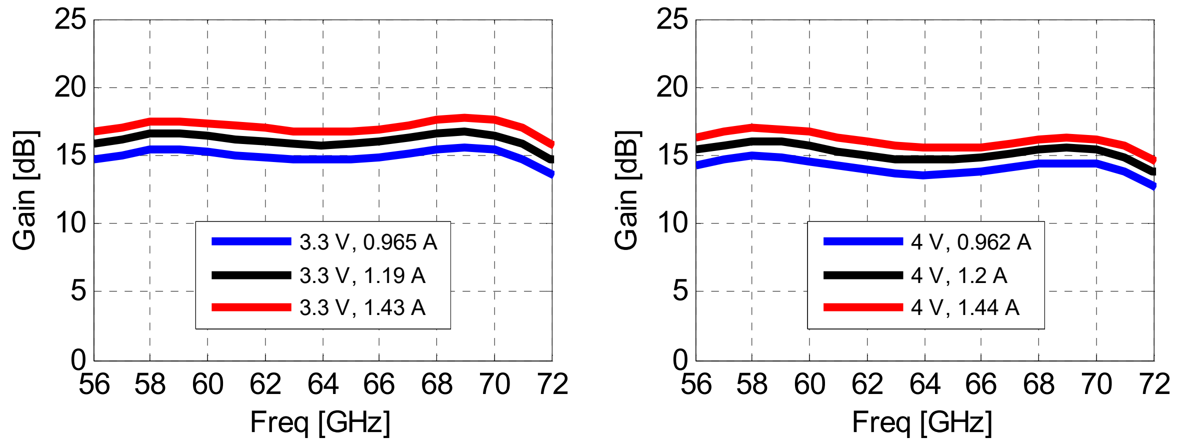


Figure 6. Gain at 3.3 V (left) and 4.0 V (right)

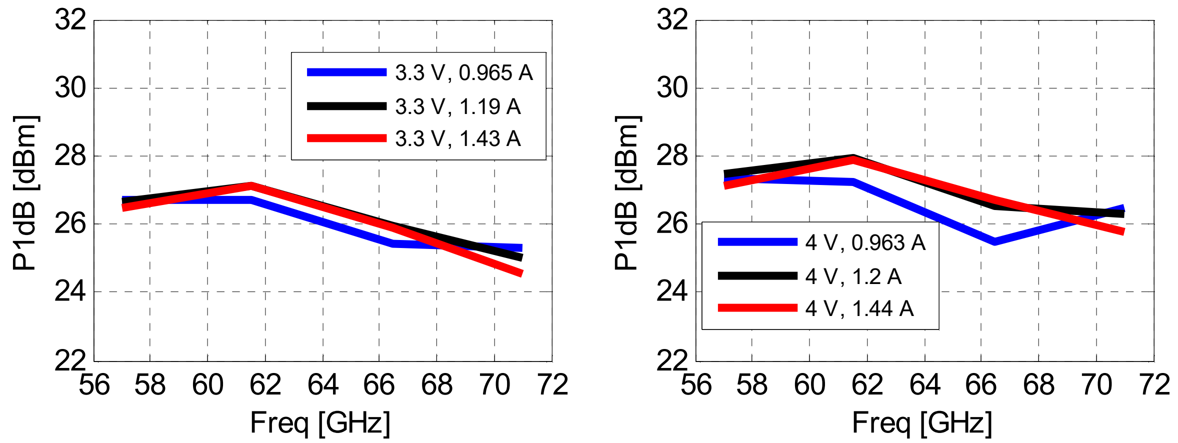


Figure 7. P1dB at 3.3 V (left) and 4.0 V (right)

Data and specification are subject to change without notice © 2020 Gotmic AB
Gotmic AB, Arvid Hedvalls Backe 4, S-411 33 Göteborg, Sweden. Tel: +46 (0) 31 184 030
www.gotmic.se/

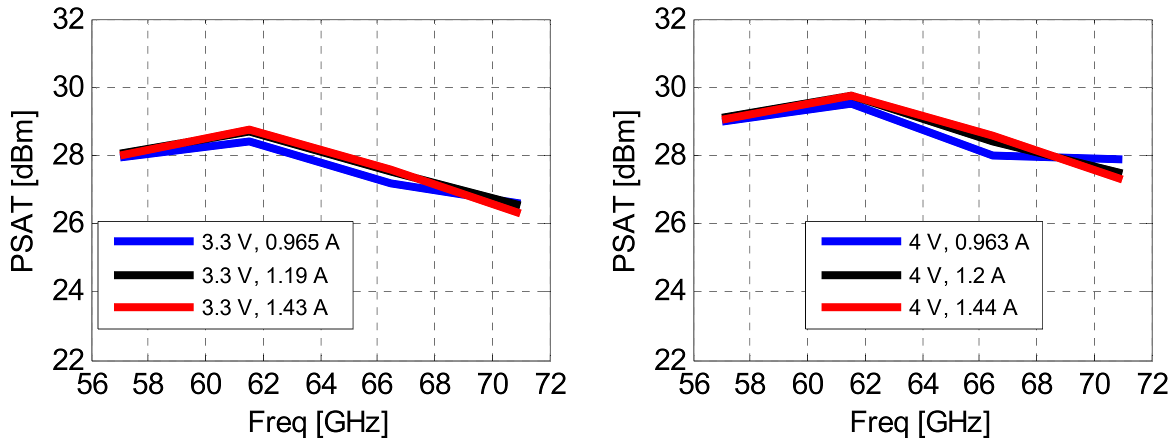


Figure 8. PSAT at 3.3 V (left) and 4.0 V (right)

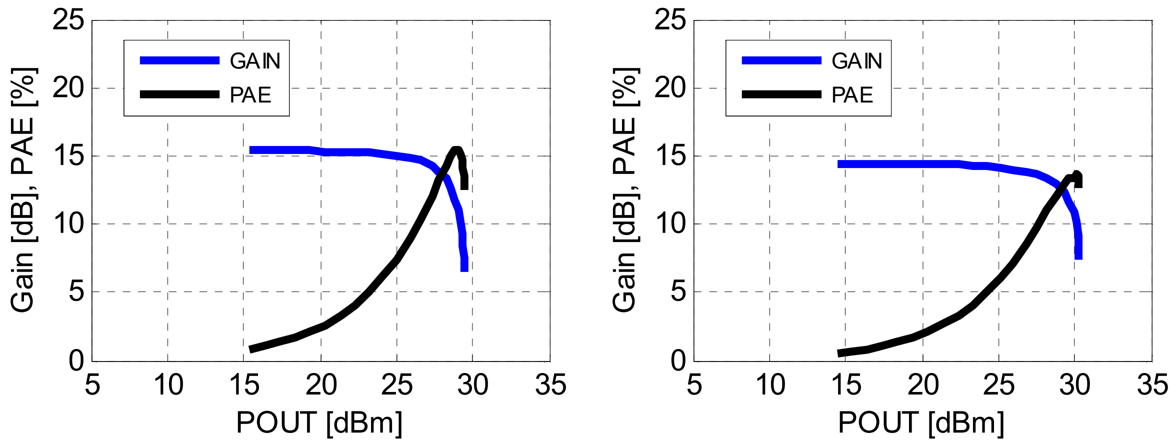


Figure 9. PAE at 3.3 V / 1.3 A (left) and 4.0 V / 1.3 A (right), 61.5 GHz

Data and specification are subject to change without notice © 2020 Gotmic AB

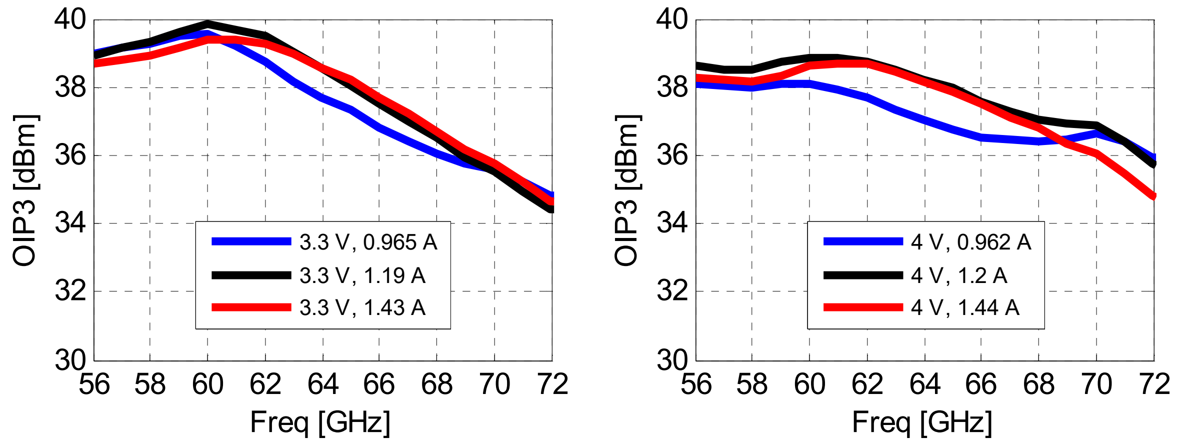


Figure 10. OIP3 at 3.3 V (left) and 4.0 V (right)

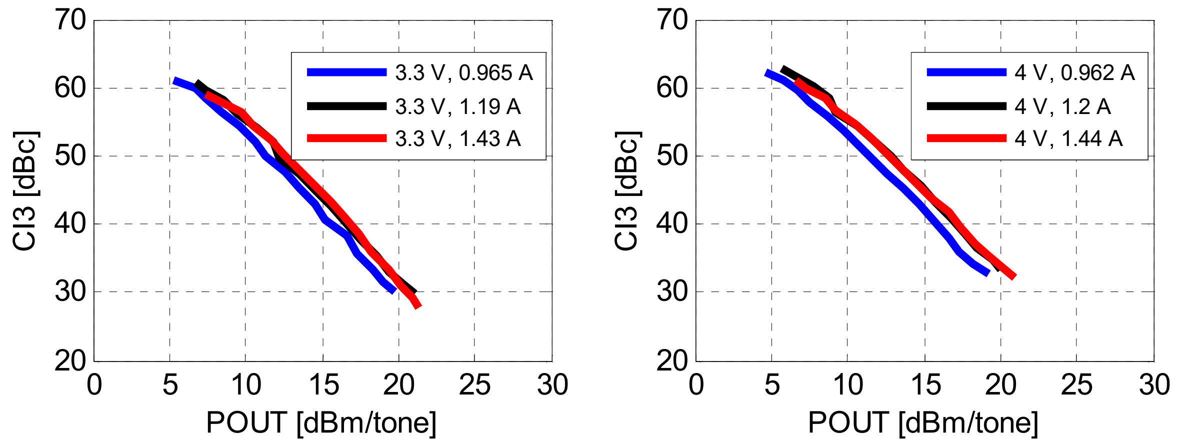


Figure 11. CI3 at 3.3 V (left) and 4.0 V (right), 61.5 GHz

Data and specification are subject to change without notice © 2020 Gotmic AB

Detector Operation

There are two identical detectors on-chip, detector A and B. Each detector can be configured for RMS power or envelope detection. Leave VREF and VDET as no-connect if not used.

To compensate for thermal variation, a reference is included on-chip. Therefore, to get a temperature compensated output, take the difference of VREF and VDET, see the recommended external detector circuit below. We recommend selecting an operational amplifier with excellent input offset voltage performance.

Detector bias is applied through VDD and a pair of resistors (R1 and R2), ideally with close to identical values. Typical bias current is 100 uA.

Envelope Detection

When configured for envelope detection it is necessary to keep transmission-line lengths to a minimum and select external components with good RF performance to support wide bandwidth baseband signals.

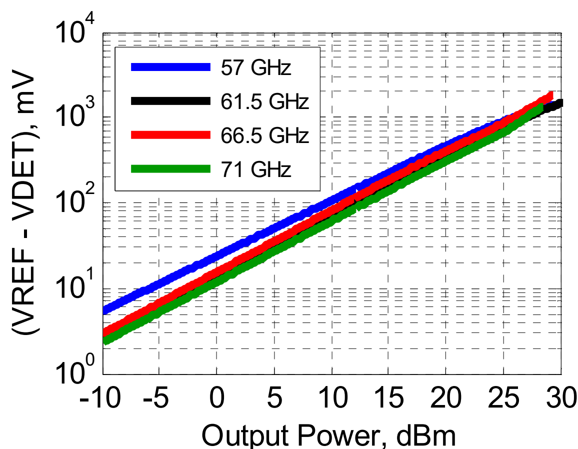
With a bias-T, which can be as simple as a shunt resistor and a series capacitor connected to VDET, the bias current is regulated with the resistor while the envelope signal can pass the capacitor. Typical bias current is 100 uA.

The reference output, VREF, is not required for envelope detection.

Typical output to a 200 Ohm load is 1.5 mVpp at -5 dBm (RMS), 12 mVpp at 5 dBm (RMS) and 52 mVpp at 15 dBm (RMS). The 3 dB bandwidth is typically 1 GHz.

Temperature Sensor

A PN-diode temperature sensor with grounded cathode is available on-chip. Typical bias current is 100 uA and can be achieved by connecting eg. a 36.5k resistor between TEMP and a +5.0 V supply. Diode voltage is 1210 mV (typ.) at +25 °C and -1.4 mV/°C.



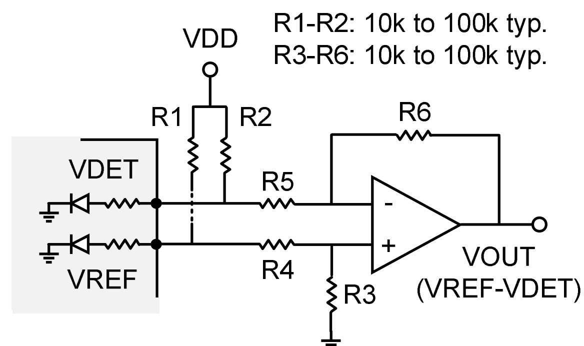


Figure 12. Detector output (left) and the external detector circuit (right)

Data and specification are subject to change without notice © 2020 Gotmic AB

Assembly Diagram

Gates and drains on side A are internally connected on-chip to the corresponding gates and drains on side B. However, it is recommended to connect drain supplies to both A and B, see assembly diagram below. Always make sure that the rated maximum drain current is never exceeded.

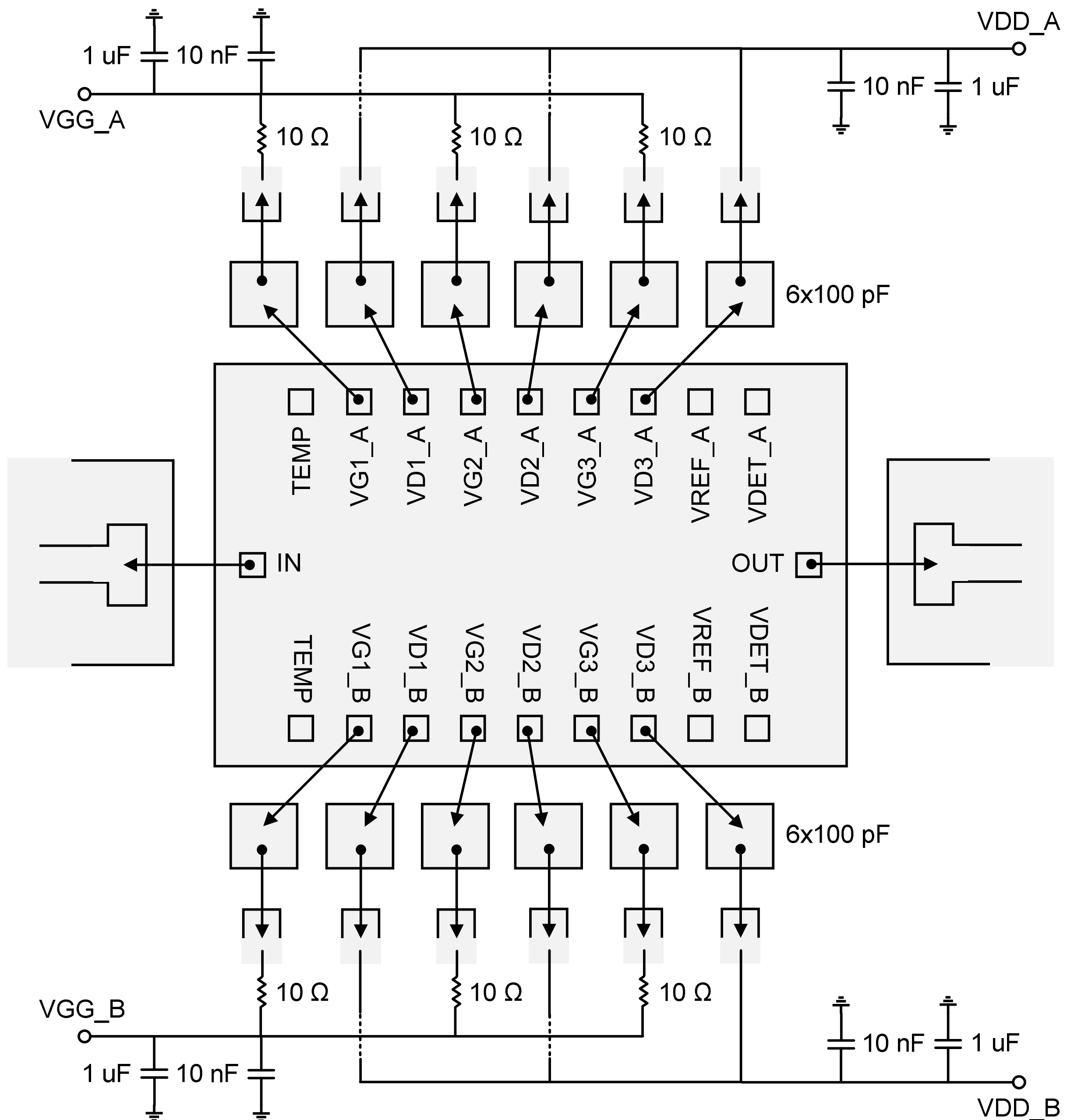


Figure 13. Assembly diagram

Data and specification are subject to change without notice © 2020 Gotmic AB

Assembly Guidelines

Mount the die to an electrically grounded plane with excellent thermal properties. Make sure the surface is clean and flat before attaching the die. Both solder and epoxy can be used, we recommend eg. CM 124-08 silver epoxy.

Bonding

The input and output is pre-matched to 50 Ohm at the pad. For optimum performance keep bond-wires as short as possible and use an external bond-wire inductance matching network. Bonding outside the area of a pad may damage the passivation layer.

DC Bypass

For stable operation locate external DC bypass capacitors near the die to reduce the bond-wire length and corresponding inductance. See assembly diagram for a recommended bypass network. Use high quality SLCs, eg. CSM-200-10X10X5-G-101-Y and low ESR ceramic or tantalum SMD capacitors.

Outline Drawing

Dimensions are in um. The MMIC thickness is 50 um. A dxf file is also available on request for use with CAD tools.

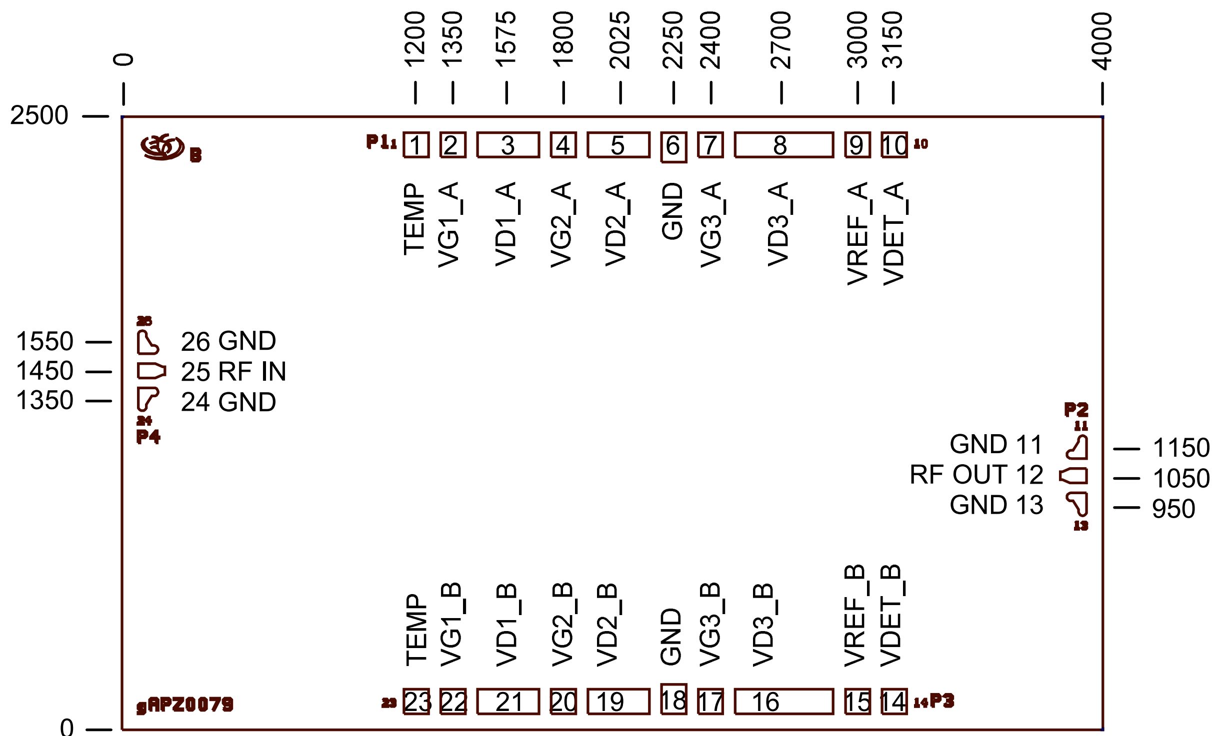


Figure 14. MMIC outline drawing