(PRELIMINARY) gAPZ0100A
W-band Medium Power Amplifier
92-100 GHz (88-104 GHz)

FEATURES

- 92-100 GHz
- 22 dBm PSAT
- 15 dB gain
- Integrated detector
- Nominal bias: 4.0 V and 325 mA
- Size: 3 x 1.2 x 0.05 mm

APPLICATIONS

- Point-to-point communication
- Radar and imaging
- Instrumentation
- Fiber over radio

DESCRIPTION

The gAPZ0100A is a bare die GaAs pHEMT four-stage power amplifier MMIC optimized for 92-100 GHz. It is ideal for W-band radar applications and long-range spectral efficient point-to-point communication.

At a nominal bias of 4.0 V and 325 mA the MMIC dissipates 1.3 W and deliver 22 dBm saturated power at 10 % PAE.

A temperature compensated detector is integrated on-chip and can be configured for RMS power or envelope detection.

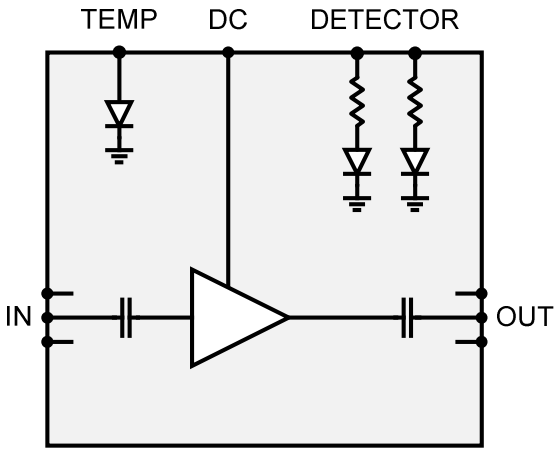

Figure 1. Circuit block diagram

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ELECTRICAL SPECIFICATIONS

Table 1. Electrical specifications, backside temperature +25 °C, nominal bias

Parameter		Min	Typ	Max	Unit
Frequency Range (performance)		92		100	GHz
Frequency Range (extended)		88		104	GHz
Gain			15		dB
Gain Temperature Slope			-0.05		dB/°C
OP1dB					dBm
PSAT (3 dB compression)			22		dBm
PAE at PSAT			10		%
OIP3					dBm
Input Return Loss			10		dB
Output Return Loss			10		dB
Detector Output at POUT *(VREF - VDET)*	-10 dBm		3		mV
	0 dBm		20		
	10 dBm		100		
	20 dBm		500		
	30 dBm		2000		
PDC (quiescent)	3.3 V / 325 mA		1073		mW
	4.0 V / 325 mA		1300		

Table 2. Absolute maximum ratings

Gate voltage (VG..)	-2.0 V
Drain voltage (VD..)	+4.5 V
Drain currents: ID1 ID2 ID3	 105 mA 140 mA 210 mA
DET, REF	1 mA
TEMP	1 mA
RF input power	+15 dBm
Junction temperature (1 million hours MTTF) *Thermal resistance (+85 °C backside temp, incl. epoxy)*	+150 °C *36 °C/W*
Operating temperature	-40 to +85 °C
Storage temperature	-65 to +150 °C

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PAD CONFIGURATION AND BIAS

Always apply the gate supplies first followed by the drain supplies. It is recommended to initially set all gates to -1.6 V and adjust the gate supplies to obtain the specified drain currents.

The typical gate voltage can vary by up to 0.2 V from what is noted. The drain currents are listed with all RF input signals off.

When gates and drains are combined external to the chip using a common gate and drain supply, adjust the common gate voltage to achieve a total drain current of 325 mA.

Table 3. Pad configuration on connector P1

Pad No.	Reference	Supply (V)	Current (mA)	Function
1	TEMP	See temperature sensor		Temperature output
2	VG1	-0.5 (typ.)		Bias
3	VD1	4.0	75	Bias
4	VG2	-0.5 (typ.)		Bias
5	VD2	4.0	100	Bias
6	GND			GND
7	VG3	-0.5 (typ.)		Bias
8	VD3	4.0	150	Bias
9	NC			
10	NC			

Table 4. Pad configuration on connector P2

Pad No.	Reference	Interface	Function
11	GND		GND
12	RF_OUT	50 Ohm, open-circuit at DC	RF output
13	GND		GND

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Table 5. Pad configuration on connector P3

Pad No.	Reference	Supply (V)	Current (mA)	Function
14	NC			
15	VDET	See detector operation		Detector output
16	GND			GND
17	VREF	See detector operation		Detector reference
18	NC			

Table 6. Pad configuration on connector P4

Pad No.	Reference	Interface	Function
19	GND		GND
20	RF_IN	50 Ohm, open-circuit at DC	RF input
21	GND		GND

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TYPICAL PERFORMANCE

Unless otherwise noted, all data presented has been obtained from on-wafer measurements, at room temperature and at nominal bias.

The two-tone RF input signal at -8 dBm/tone has a separation frequency of 50 MHz.

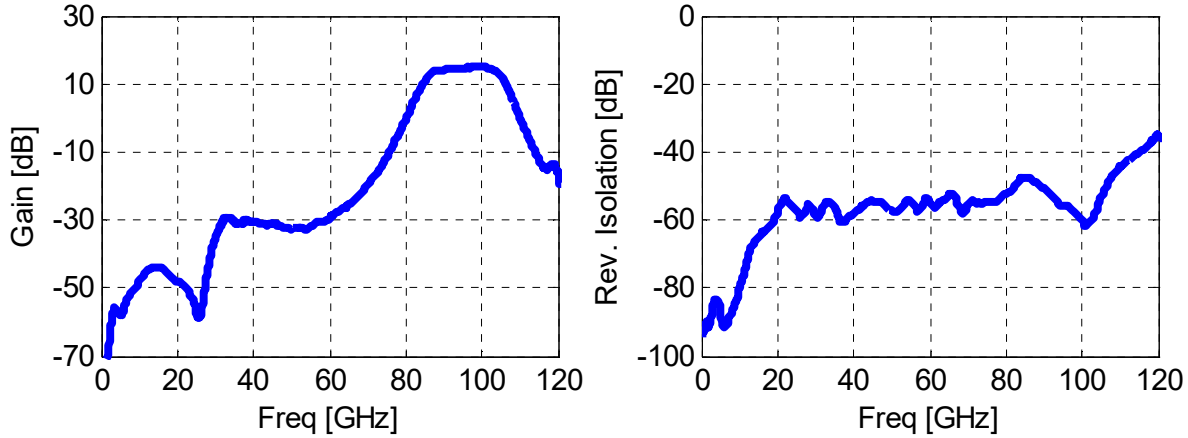

Figure 2. Gain (left) and reverse isolation (right)

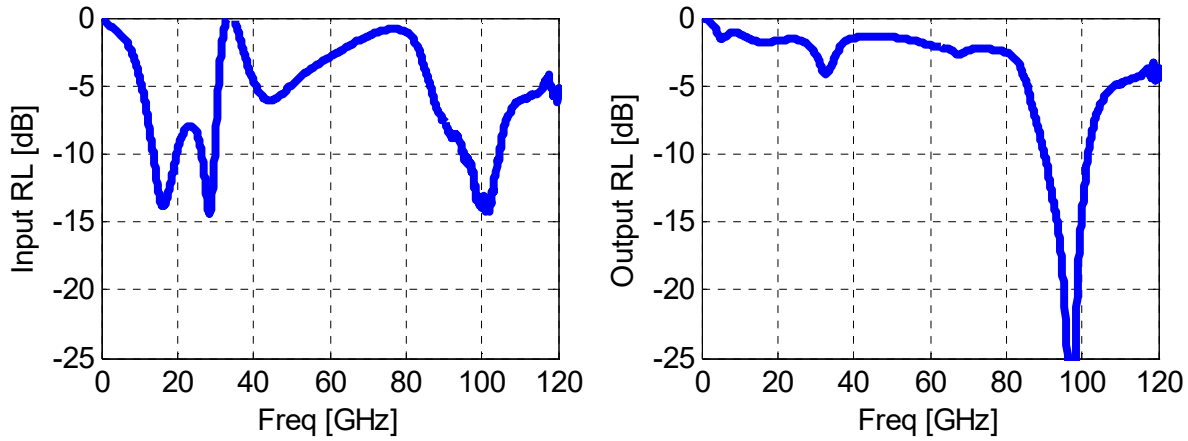

Figure 3. Input (left) and output return loss (right)

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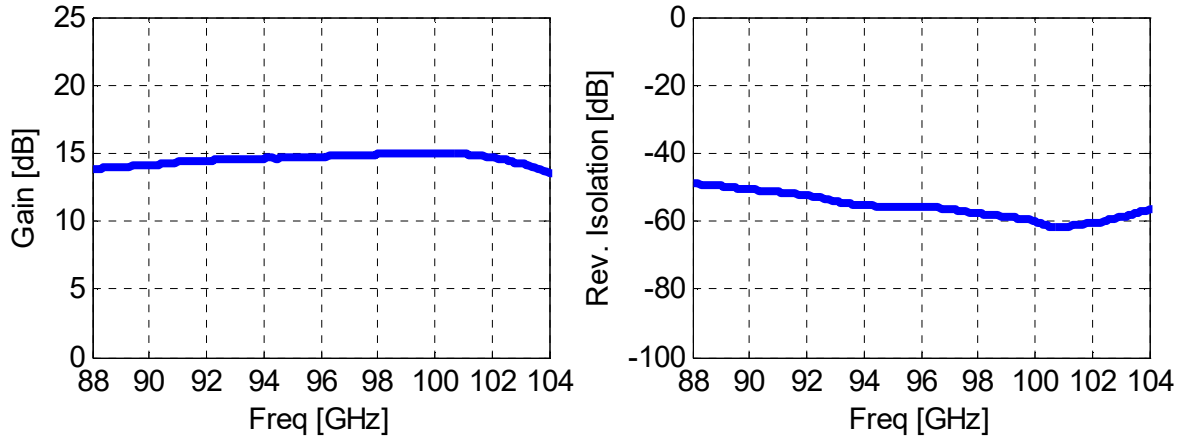

Figure 4. In-band gain (left) and reverse isolation (right)

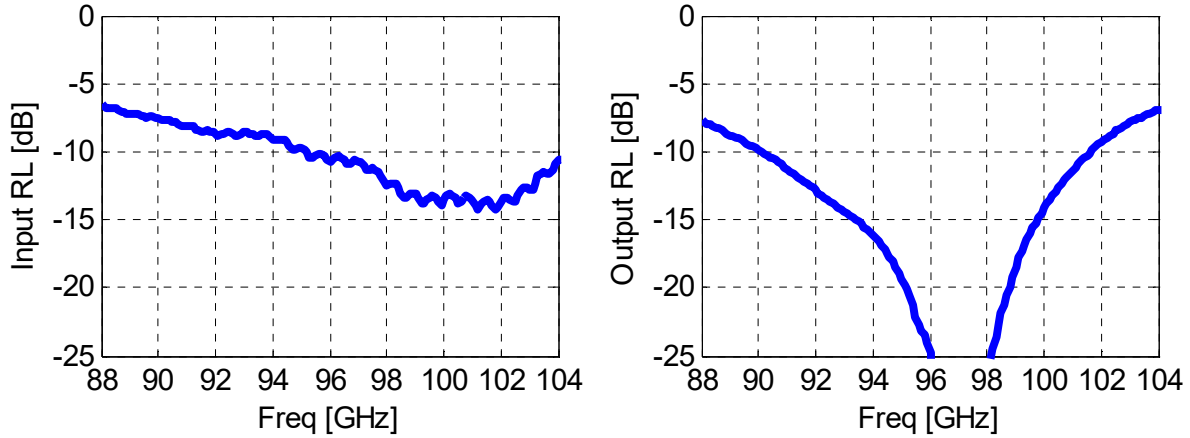

Figure 5. In-band input (left) and output return loss (right)

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Detector Operation

The detector can be configured for RMS power or envelope detection. Leave VREF and VDET as no-connect if not used.

To compensate for thermal variation, a reference is included on-chip. Therefore, to get a temperature compensated output, take the difference of VREF and VDET, see the recommended external detector circuit below. We recommend selecting an operational amplifier with excellent input offset voltage performance.

Detector bias is applied through VDD and a pair of resistors (R1 and R2), ideally with close to identical values. Typical bias current is 100 uA.

Envelope Detection

When configured for envelope detection it is necessary to keep transmission-line lengths to a minimum and select external components with good RF performance to support wide bandwidth baseband signals.

With a bias-T, which can be as simple as a shunt resistor and a series capacitor connected to VDET, the bias current is regulated with the resistor while the envelope signal can pass the capacitor. Typical bias current is 100 uA.

The reference output, VREF, is not required for envelope detection.

Typical output to a 200 Ohm load is 1.5 mVpp at -5 dBm (RMS), 12 mVpp at 5 dBm (RMS) and 52 mVpp at 15 dBm (RMS). The 3 dB bandwidth is typically 1 GHz.

Temperature Sensor

A PN-diode temperature sensor with grounded cathode is available on-chip. Typical bias current is 100 uA and can be achieved by connecting eg. a 36.5k resistor between TEMP and a +5.0 V supply. Diode voltage is 1210 mV (typ.) at +25 °C and -1.4 mV/°C.

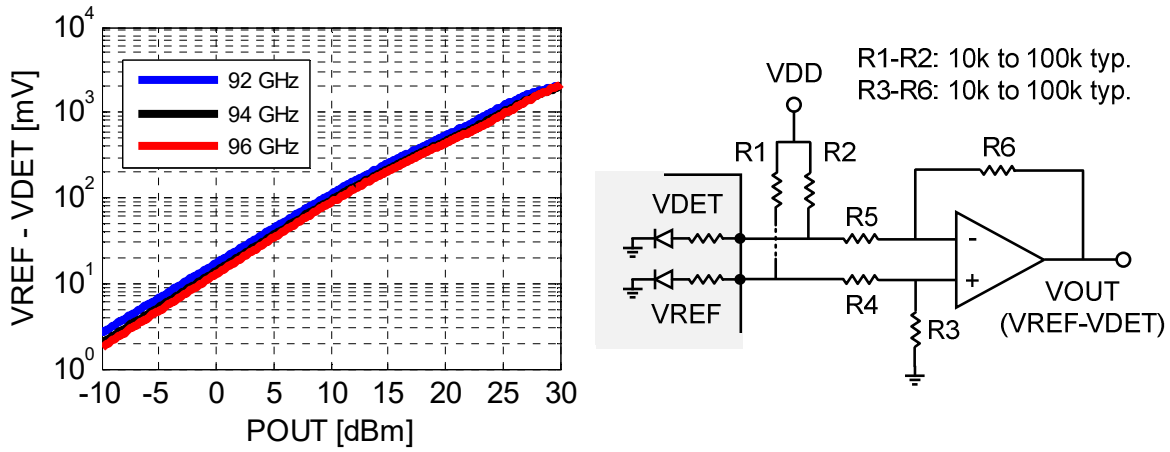

Figure 6. Detector output (left) and the external detector circuit (right)

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ASSEMBLY DIAGRAM

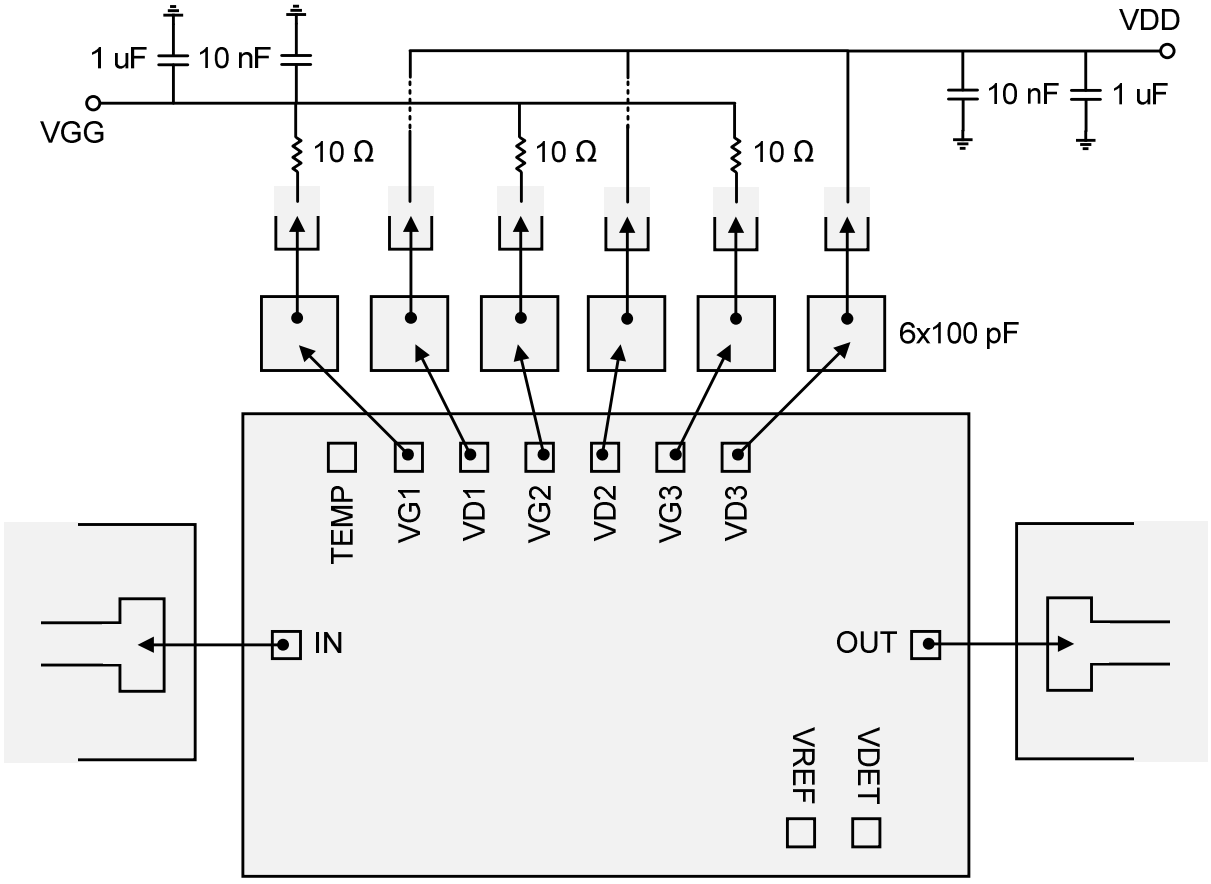

Figure 7. Assembly diagram

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Assembly Guidelines

Mount the die to an electrically grounded plane with excellent thermal properties. Make sure the surface is clean and flat before attaching the die. Both solder and epoxy can be used, we recommend eg. CM 124-08 silver epoxy.

Bonding

The input and output is pre-matched to 50 Ohm at the pad. For optimum performance keep bond-wires as short as possible and use an external bond-wire inductance matching network. Bonding outside the area of a pad may damage the passivation layer.

DC Bypass

For stable operation locate external DC bypass capacitors near the die to reduce the bond-wire length and corresponding inductance. See assembly diagram for a recommended bypass network. Use high quality SLCs, eg. CSM-200-10X10X5-G-101-Y and low ESR ceramic or tantalum SMD capacitors.

Outline Drawing

Dimensions are in um. The MMIC thickness is 50 um. A dxf file is also available on request for use with CAD tools.

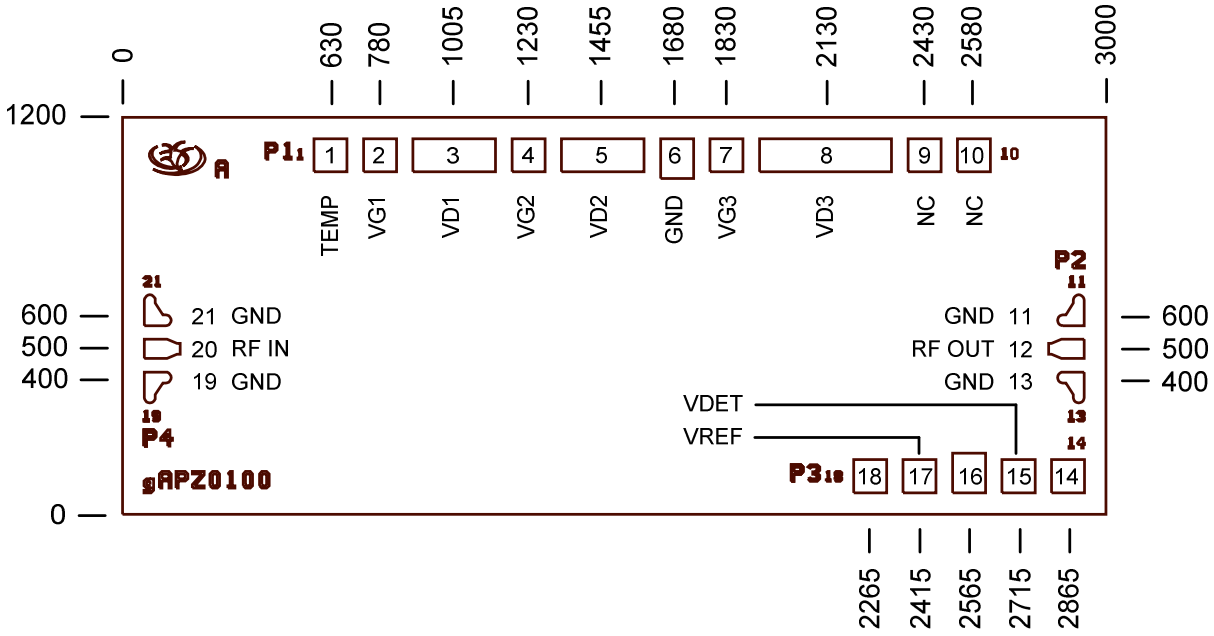

Figure 8. MMIC outline drawing

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