gRSC0016 B
V-band RX MMIC
57-66 (52 – 72) GHz

Features

- V-band coverage
- 15 dB conversion gain
- 4 dB NF
- Direct or IF down conversion

Typical applications

- V-band point-to-point radio
- Test and measurement
- Sensing

Description

gRSC0016 is a complete highly integrated receiver for V-band radio applications. The multifunctional chip has a x6 frequency multiplier, mixer and low noise amplifier integrated on the chip. The differential IQ mixer is highly linear with low conversion loss. The frequency multiplier has low spuriouses and flat output power throughout the entire V-band. The LNA has high gain, low noise figure and being linear, making the receiver suitable for 64+ QAM modulation.

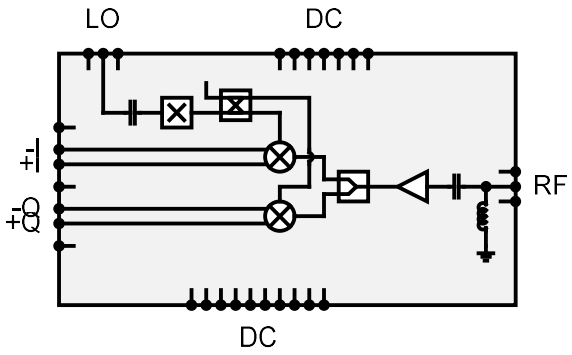

Figure 1. Block diagram of the receiver.

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Electrical performance

Table 1. Electrical performance T_A=25°C

Parameter	Min	Typ	Max	Unit
RF frequency	57 (52)		66 (72)	GHz
IF frequency	DC		12	GHz
LO input frequency	9.5		11	GHz
LO input power		10		dBm
LO multiplication factor		6		
Conversion gain[1]		15		dB
LO power at RF port			Tbd	dBm
Image Rejection Ratio (IRR)	20			dB
Input referred P1dB	tbd			dBm
OIP3	10	13		dBm
IIP3[2]		-5		dBm
OIP2[3]		22		dBm
IIP2[3]		7		dBm
NF[4]		4		dB
RF return loss	7			dB
IF return loss	tbd			dB
LO return loss	10			dB
Power consumption		600		mW

[1] Gain temperature coefficient is (tbd) dB/C.

[2] IIP3 can be improved with reduced gain of the LNA.

[3] IP2 can be increased significantly using I+, I-, Q+ and Q- DC offset voltages. It can also be surpressed using a differential IF amplifier since the IM2 product is in phase at the I and Q pairs.

[4] The receiver noise figure is calculated using the measurement data from the LNA.

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Measured performance

Measurements have been performed on-wafer with RF input power = -25 dBm/tone, tone separation = 10 MHz, IF frequency = 1 GHz, T_A = 25°C and typical bias settings if not specified differently.

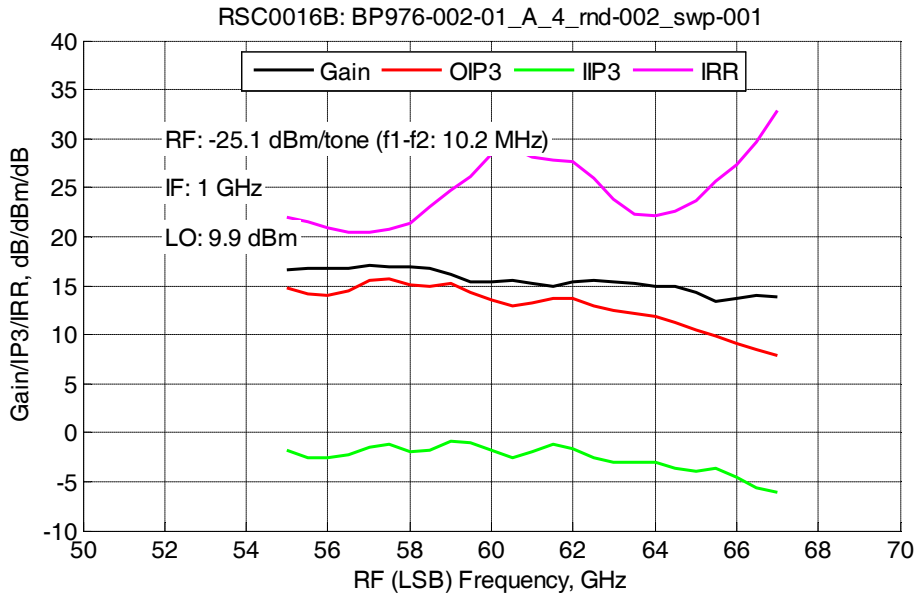

Figure 2: Typical gain, IP3 and IRR performance.

Settings

The bias sequence is to first apply all gates (VG…) followed by all drains (VD…). The typical drain current should be obtained by adjusting the corresponding gate. All stated drain currents are when all input signals are off.

Table 2. Electrical settings on connector P1

Connector P1	Pad No.	Settings	Function
GND	1		Ground
LO	2	Z_0 = 50 Ohm, AC coupled	Input
GND	3		Ground

Table 3. Electrical settings on connector P2

Connector P2	Pad No.	Bias settings (V / mA)			Function
		Min	Typ	Max	
NC	1				NC
VD_AMP	2	3.2	3.3 / 80	3.4 / 180[5]	Input
VG_AMP	3	-0.7	-0.5	-0.3	Input
GND	4				Ground
VD_X2	5	3.2	3.3 / 5	3.4 / 605	Input
VG_X2	6	-1.1	-0.9	-0.7	Input
VD_X3	7	3.2	3.3 / 50	3.4 / 80[5]	Input
VG_X3	8	-0.7	-0.5	-0.3	Input
NC	9				NC
NC	10				NC

Table 4. Electrical settings on connector P3

Connector P3	Pad No.	Settings	Function
GND	1		Ground
I+	2	Z_0 = 100 Ohm differential impedance, DC coupled	Output
I-	3		Output
GND	4		Ground
Q+	5	Z_0 = 100 Ohm differential impedance, DC coupled	Output

[5] Maximum current level before damage. Not for improved performance.

Q-	6		Output
GND	7		Ground

Table 5. Electrical settings on connector P4

Connector P4	Pad No.	Bias settings (V / mA)			Function
		Min	Typ	Max	
NC	1				NC
NC	2				NC
VG1_LNA	3	-0.7	-0.5	-0.3	Input
VD1_LNA	4	1.1	1.2 / 10	1.3 / 40[5]	Ground
GND	5				Input
VG2_LNA	6	-0.7	-0.5	-0.3	Input
VD2_LNA	7	1.9	2.0 / 50	2.1 / 140[5]	Input
VG_MIX	8	-0.9	-0.7	-0.5	Input
NC	9				NC

Table 6. Electrical settings on connector P5

Connector P5	Pad No.	Settings	Function
GND	1		Ground
RF	2	Z_0 = 50 Ohm, AC coupled	Input
GND	3		Ground

Table 7. Absolute Maximum Ratings

Gate-source voltage	-2 to +0.7 V
Drain-source voltage	4.5 V
Gate-drain breakdown voltage	8 V
RF in	+7 dBm
LO input power	+15 dBm
Operating temperature	-40 to + 85°C
Storage temperature	-65 to +150°C

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Outline drawing

Mechanical drawing with pad locations is also available in dxf-file format on the web. Substrate thickness is 50 µm (GaAs).

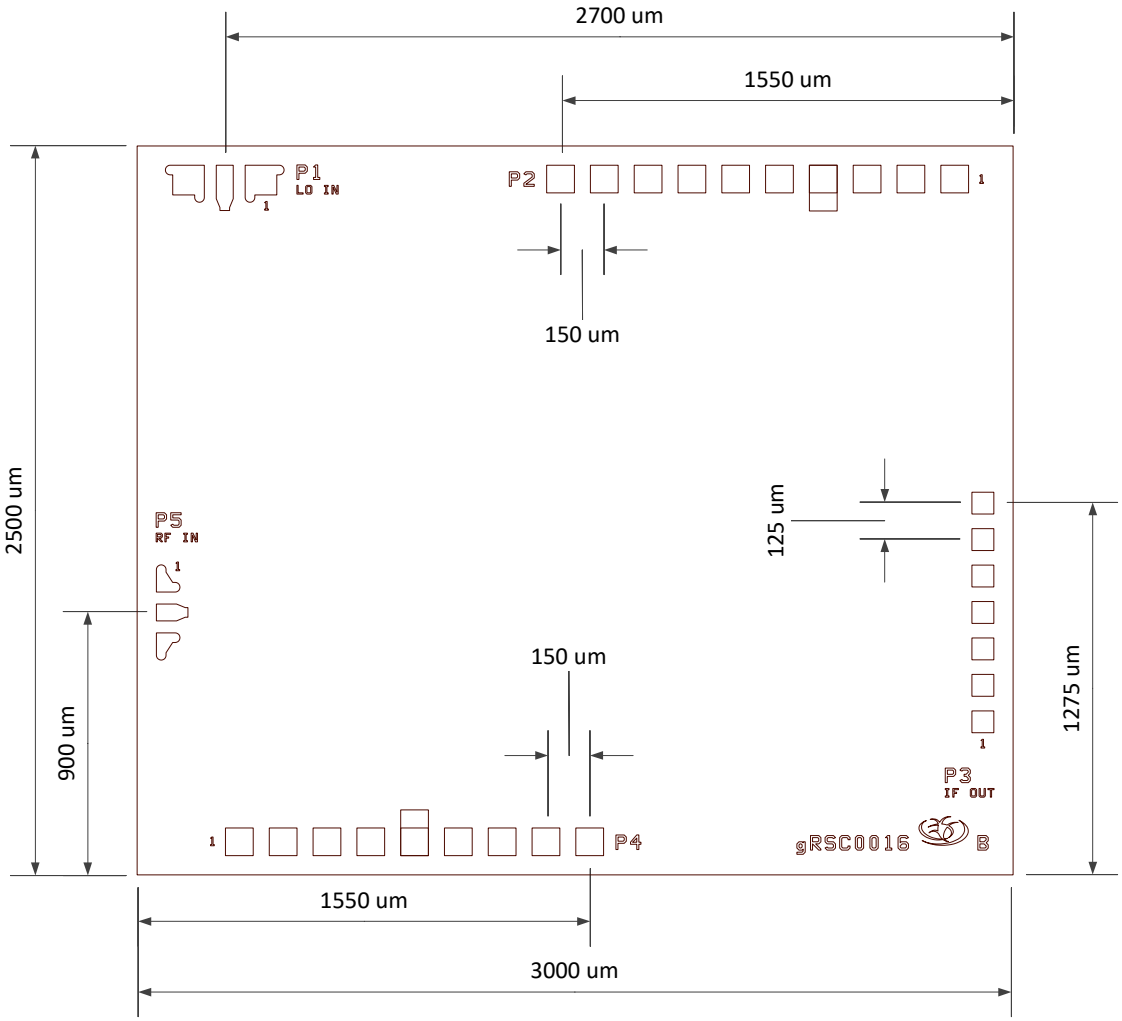

Figure 3. Outline drawing of the MMIC. Dimensions are in um.

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